1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
06		281154	ENGINEERING RELEASED	06/20/03	?

Q16 DVT
WALDORF

Fri Jun 20 16:33:16 2003

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11	400PIN STACKED DDR SODIMM CONNECTOR
12	INTREPID AGP 4X/PCI
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BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6338	1	SCHEM,Q16,WALDORF	SCH1	
820-1441	1	PCBF,Q16,WALDORF	PCB1	
065-3951	1	CMNPRTS,Q16,WALDORF	DMS1	DMS630-4285&DMS630-4721
065-3952	1	SELPRTS,Q16,WALDORF,BTR	DMS2	DMS630-4285
065-4479	1	SELPRTS,Q16,WALDORF,BST	DMS3	DMS630-4721

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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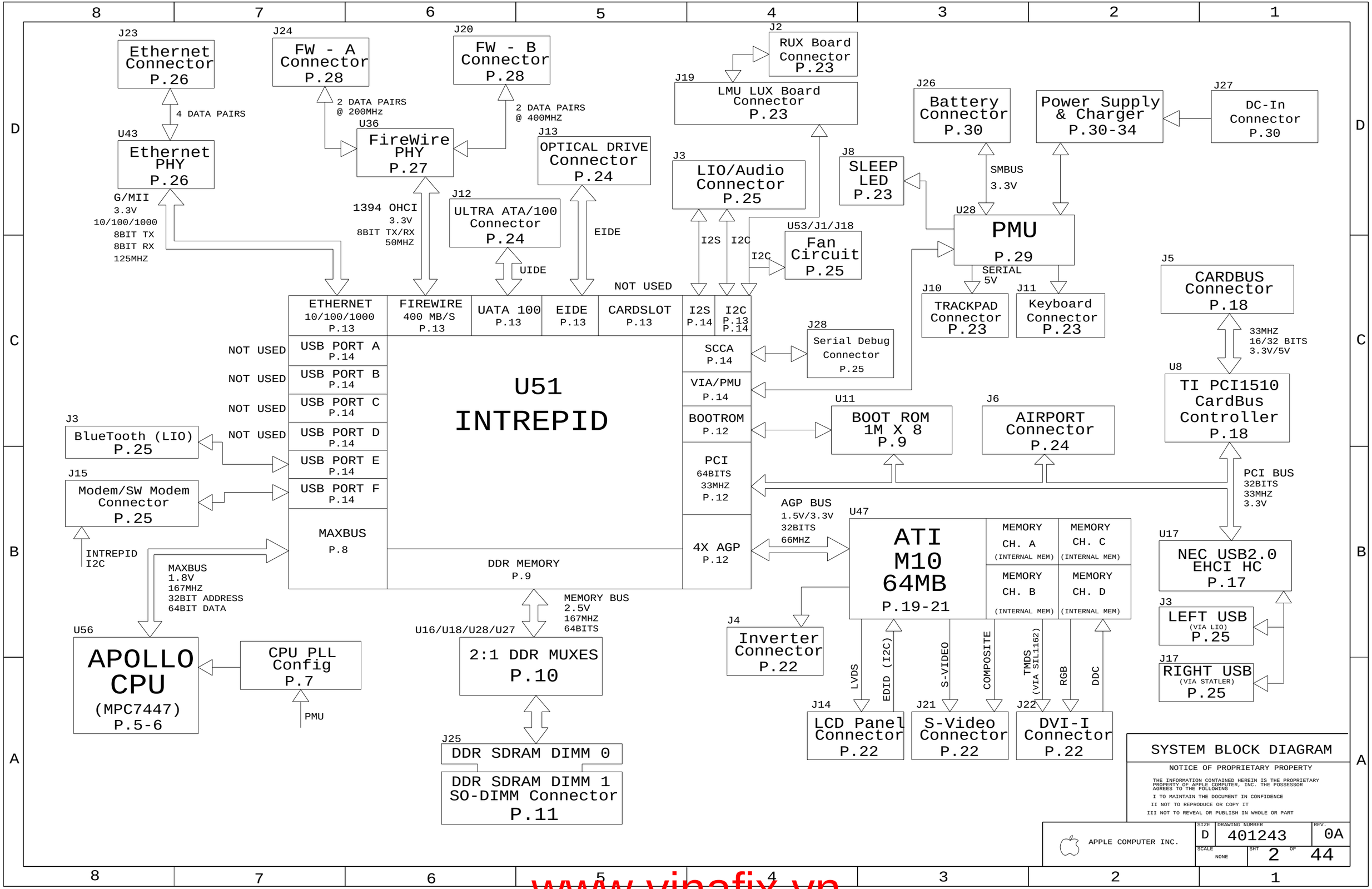
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TITLE
SCHEM,Q16,WALDORF

DRAWING NUMBER 401243 REV. 0A

SHT 1 OF 44

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POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 30

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF
PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 31
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

14V_PBUS

+3V_PMU LDO PG 31

+BATT

+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 32
VCC
STBYMD
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 31

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 30

+BATT

3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 30

+PBUS

DC/DC (LTC3411)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 34

+1.8V_MAIN
MAXBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN
INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC
VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING
RUN/SS
PG 20

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK
D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

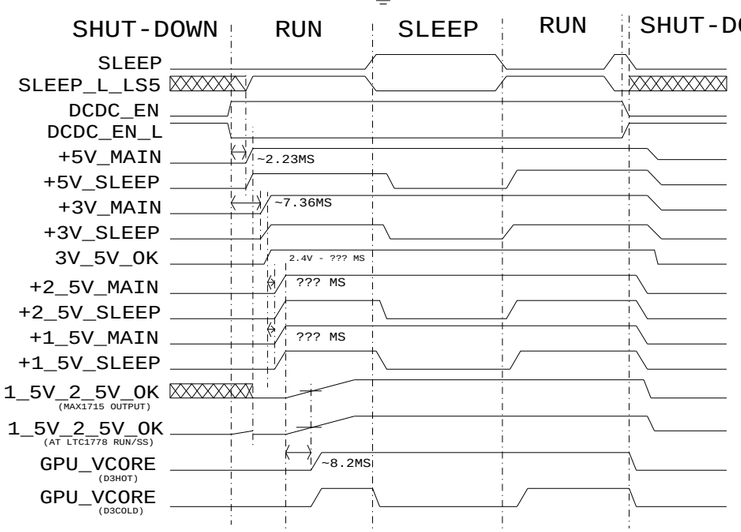
DCDC_EN
SLEEP
MAXBUS SEQUENCING

+PBUS

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33

CPU_VCORE (+1.385V)



POWER BLOCK DIAGRAM

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SCALE	SHT	OF
NONE	3	44

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PCB SPECS

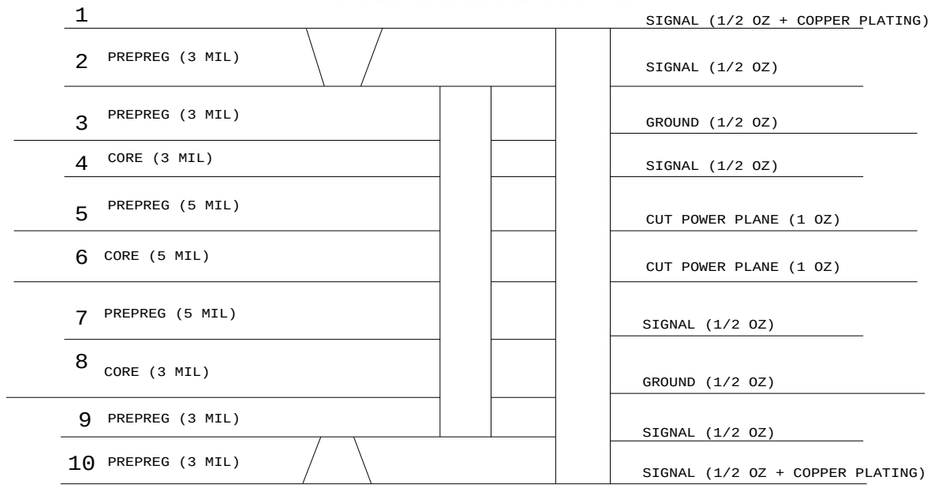
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA



BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA

ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R10 DVI 1394 — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER

SH1 OG-503040 SHLD-SM — CHGND3

MECH. HOLES

ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301_SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302_SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10_SPN NO_TEST=TRUE

GROUND VIAS

ZT76, ZT28, ZT72, ZT69, ZT68, ZT64, ZT61, ZT38, ZT39, ZT40, ZT41, ZT46, ZT71, ZT78, ZT80 HOLE-VIA-20R10

ZT50, ZT51, ZT52, ZT53, ZT57, ZT60, ZT82, ZT22, ZT17, ZT35, ZT45, ZT79, ZT81, ZT83, ZT49 HOLE-VIA-20R10

ZT48, ZT47, ZT54, ZT55, ZT56, ZT84, ZT5, ZT15, ZT44, ZT4, ZT8, ZT6, ZT32, ZT3, ZT10 HOLE-VIA-20R10

ZT11, ZT34, ZT20, ZT43, ZT70, ZT2, ZT9, ZT75, ZT73, ZT63, ZT77, ZT66, ZT62, ZT65, ZT13 HOLE-VIA-20R10

ZT25, ZT19, ZT24, ZT67, ZT37, ZT29, ZT31, ZT1, ZT14, ZT12, ZT27, ZT26, ZT30, ZT33, ZT18 HOLE-VIA-20R10

BOARD INFORMATION

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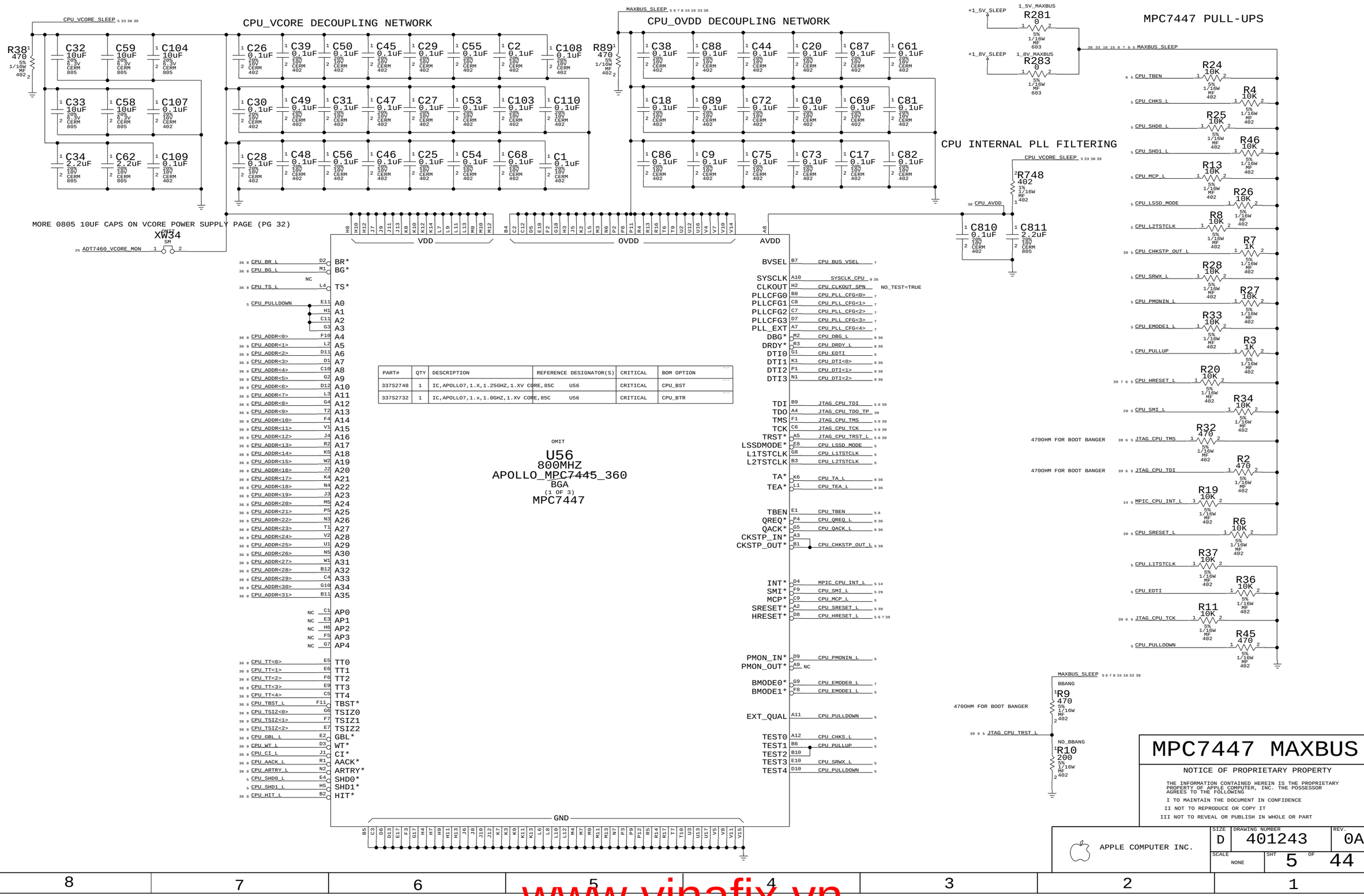
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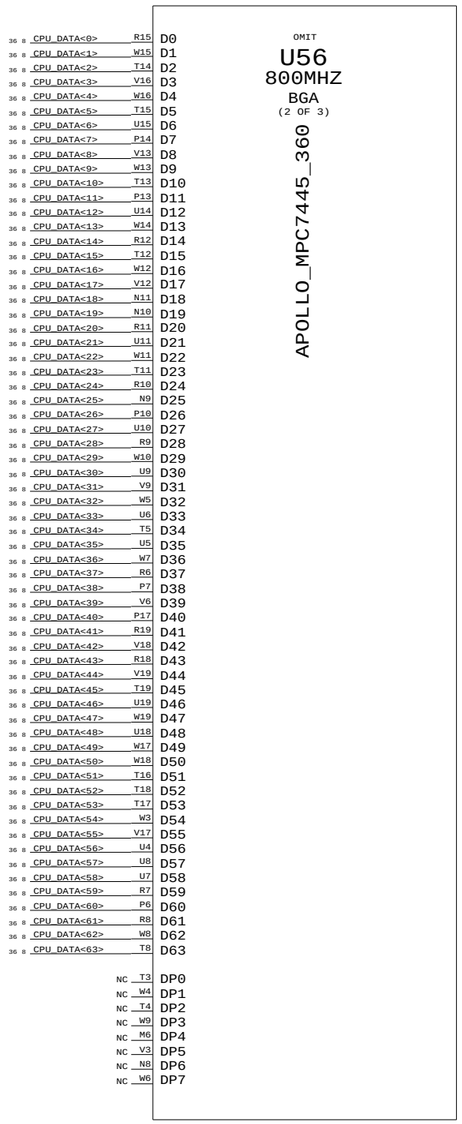
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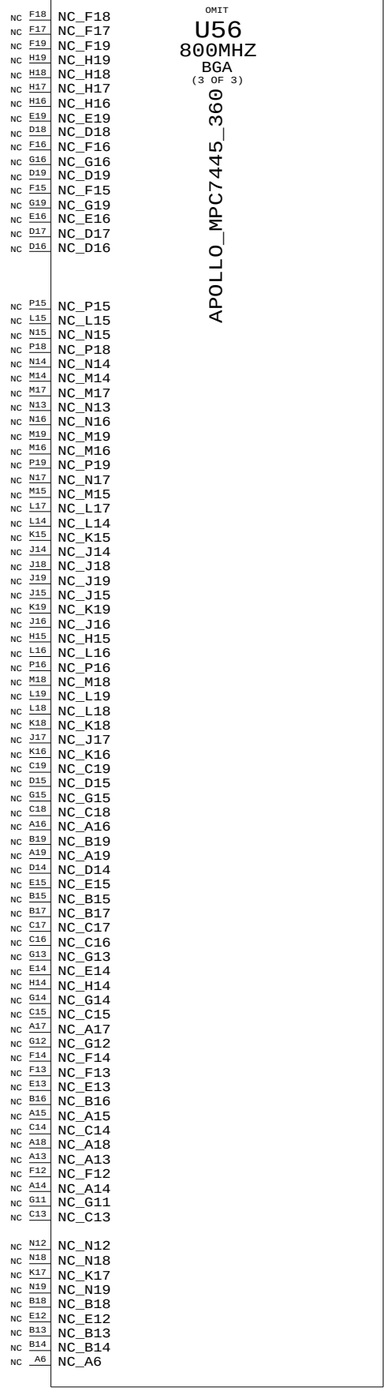
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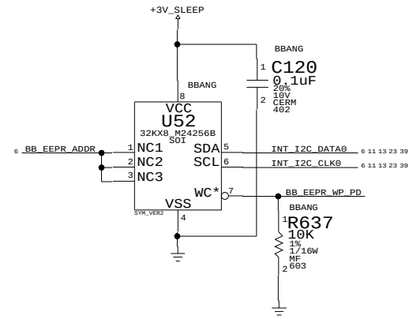
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2748	1	IC,APOLLO7,1.X,1.25GHZ,1.XV CORE,85C	U56	CRITICAL	CPU_BST
337S2732	1	IC,APOLLO7,1.X,1.0GHZ,1.XV CORE,85C	U56	CRITICAL	CPU_BTR

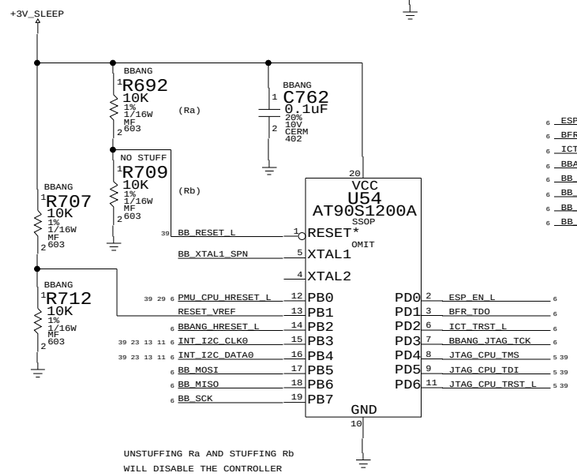
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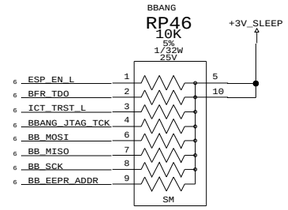




BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

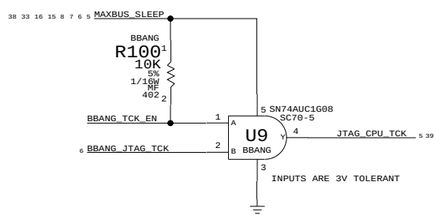


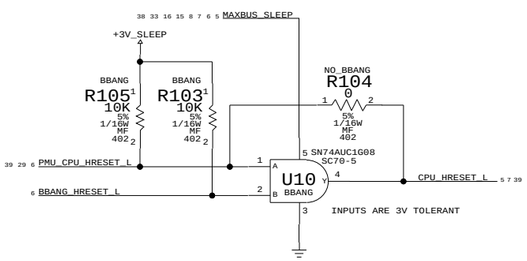




UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	000-6240 FW GT4 BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

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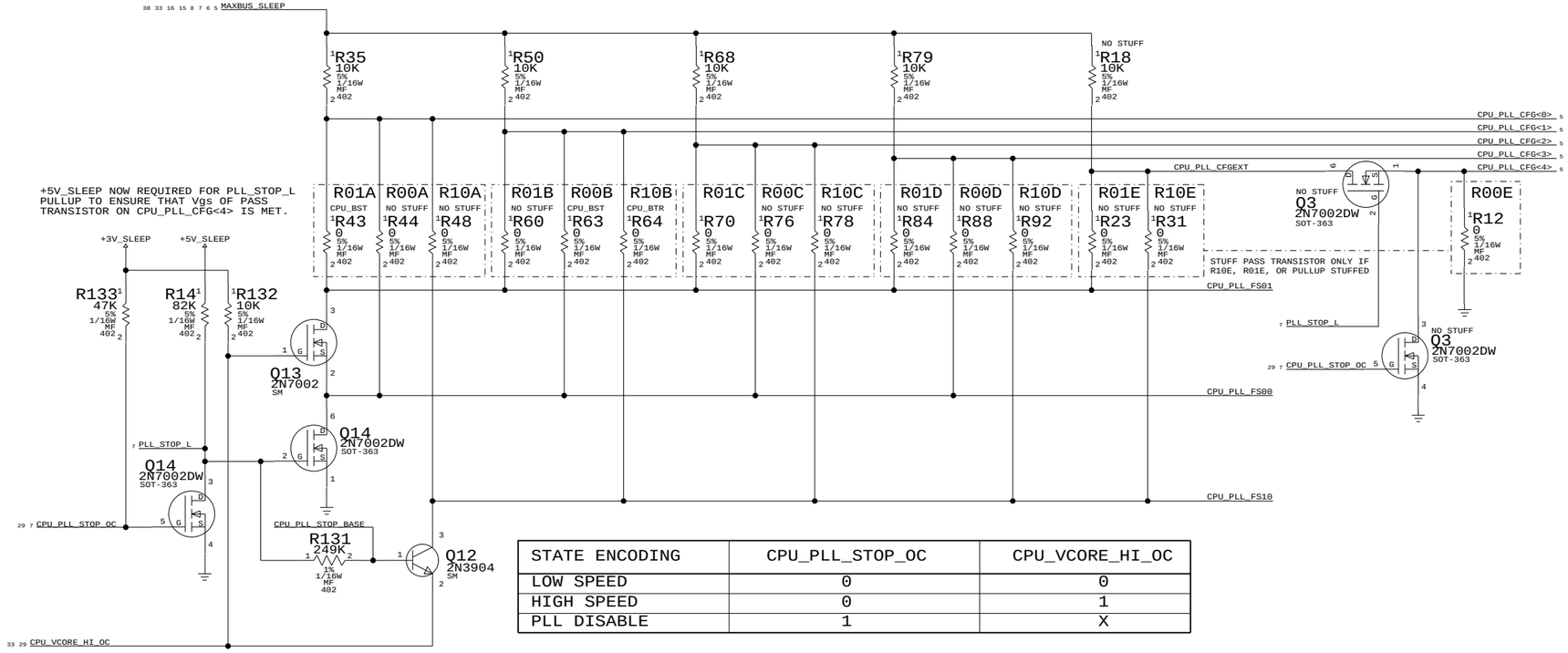
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CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

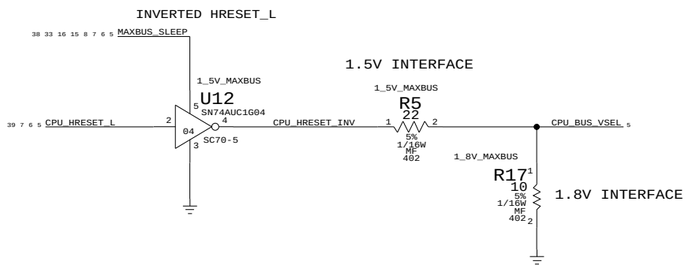
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF R640[1] 10K	NO STUFF R639[1] 10K	NO STUFF R638[1] 10K	NO STUFF R666[1] 10K	R622[1] 10K	R619[1] 10K	R618[1] 10K	R653[1] 10K
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
0: TDO output (default) 1: TDI output	0: Disable JTAG 1: Active	0: Disable Analyzer clk 1: Active	0: Disable Pull down 1: Active low	Spare	Spare	Spare	Spare

R621[1] 10K	R620[1] 10K	R652[1] 10K	R650[1] 10K				
CPU_DATA<39>	CPU_DATA<38>	CPU_DATA<37>	CPU_DATA<36>				
0: Disable Pull up 1: Active low	Spare	Spare	Spare	Spare			

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF R641[1] 10K	SSCG R665[1] 10K	NO STUFF R664[1] 10K	NO_SSCG R693[1] 10K	NO STUFF R694[1] 10K	NO STUFF R699[1] 10K		
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>

R648[1] 10K	R677[1] 10K	R623[1] 10K	NO_SSCG R651[1] 10K	R649[1] 10K	SSCG R678[1] 10K	R679[1] 10K	R684[1] 10K
Spare	Spare	BIT2	BIT1	BIT0	0: Internal Spread on 1: Active	0: PCI1 Source Clock (no spread) 1: PLL3	0: PCI0 Source Clock (no spread) 1: PLL4

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

SSCG R696[1] 10K	SSCG R695[1] 10K	NO STUFF R667[1] 10K	NO STUFF R668[1] 10K	NO STUFF R643[1] 10K	NO STUFF R642[1] 10K	R698[1] 10K	
CPU_DATA<48>	CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>

NO_SSCG R681[1] 10K	NO_SSCG R680[1] 10K	NO STUFF R654[1] 10K	R655[1] 10K	R625[1] 10K	R624[1] 10K	NO STUFF R683[1] 10K	R626[1] 10K
0: Disable Buf_Ref clk OutEnable_h 1: Active	0: PLL5 4xtSrc 1: External source	0: Disable BOOTROM on IDE/CardSlot 1: BOOTROM on PCI1	OBSOLETE (Should remain high)	0: Disable 1394b workaround 1: TI 1394b workaround	BIT2	BIT1	BIT0 Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7
C187 0.22uF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6)

U51 INTREPID-REV2.1 BGA

(1 OF 9) CRITCAL

CPU_BR_L	E29	BR INPUT
CPU_BG_L	E26	BG NO BUS KEEPER
CPU_TS_L	B27	TS NO BUS KEEPER
CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31
CPU_CI_L	G26	CI
CPU_GBL_L	A29	GBL
CPU_TBST_L	A28	TBST
CPU_TSIZ<0>	G24	TSIZ_0
CPU_TSIZ<1>	H24	TSIZ_1
CPU_TSIZ<2>	D26	TSIZ_2
CPU_TT<0>	E25	TT_0
CPU_TT<1>	G25	TT_1
CPU_TT<2>	B28	TT_2
CPU_TT<3>	D27	TT_3
CPU_TT<4>	J25	TT_4
CPU_WT_L	D28	WT
CPU_AACK_L	B29	AACK NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT INPUT - PU
CPU_QREQ_L	A32	QREQ INPUT - PD
CPU_QACK_L	G27	QACK NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
INT_SUSPEND_ACK_L	AM8	SUSPENDACK

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

INT_CPUFB_IN	J24	CPU_FB_IN
INT_CPUFB_OUT	H16	CPU_FB_OUT NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK
CPU_CLK_EN	AH9	INPUT - PU STOPCPUCLK
INTREPID_ACS_REF	H13	NO BUS KEEPER - ? ACS_REF
SYSCLK_CPU	J15	NO BUS KEEPER - ? CPU_CLK
CPU_TBEN	A31	NO BUS KEEPER - PU TBEN

INTREPID OUTPUTS HIGH BY DEFAULT
NO BUS KEEPER - PU

H25 VSSA_7 (PLL6)

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>	6 36
D_1	G12	CPU_DATA<1>	6 36
D_2	E11	CPU_DATA<2>	6 36
D_3	H11	CPU_DATA<3>	6 36
D_4	B9	CPU_DATA<4>	6 36
D_5	B8	CPU_DATA<5>	6 36
D_6	A9	CPU_DATA<6>	6 36
D_7	A8	CPU_DATA<7>	6 36
D_8	E12	CPU_DATA<8>	6 36
D_9	D11	CPU_DATA<9>	6 36
D_10	B10	CPU_DATA<10>	6 36
D_11	J13	CPU_DATA<11>	6 36
D_12	A10	CPU_DATA<12>	6 36
D_13	D12	CPU_DATA<13>	6 36
D_14	E13	CPU_DATA<14>	6 36
D_15	G13	CPU_DATA<15>	6 36
D_16	B11	CPU_DATA<16>	6 36
D_17	D13	CPU_DATA<17>	6 36
D_18	A11	CPU_DATA<18>	6 36
D_19	G14	CPU_DATA<19>	6 36
D_20	H14	CPU_DATA<20>	6 36
D_21	E14	CPU_DATA<21>	6 36
D_22	B12	CPU_DATA<22>	6 36
D_23	G15	CPU_DATA<23>	6 36
D_24	B13	CPU_DATA<24>	6 36
D_25	H15	CPU_DATA<25>	6 36
D_26	D14	CPU_DATA<26>	6 36
D_27	B14	CPU_DATA<27>	6 36
D_28	A12	CPU_DATA<28>	6 36
D_29	G16	CPU_DATA<29>	6 36
D_30	E15	CPU_DATA<30>	6 36
D_31	J16	CPU_DATA<31>	6 36
D_32	D15	CPU_DATA<32>	6 8 36
D_33	A14	CPU_DATA<33>	6 8 36
D_34	A13	CPU_DATA<34>	6 8 36
D_35	D16	CPU_DATA<35>	6 8 36
D_36	E16	CPU_DATA<36>	6 8 36
D_37	G17	CPU_DATA<37>	6 8 36
D_38	B15	CPU_DATA<38>	6 8 36
D_39	H17	CPU_DATA<39>	6 8 36
D_40	A15	CPU_DATA<40>	6 8 36
D_41	B16	CPU_DATA<41>	6 8 36
D_42	E17	CPU_DATA<42>	6 8 36
D_43	A16	CPU_DATA<43>	6 8 36
D_44	J18	CPU_DATA<44>	6 8 36
D_45	H18	CPU_DATA<45>	6 8 36
D_46	D17	CPU_DATA<46>	6 8 36
D_47	G18	CPU_DATA<47>	6 8 36
D_48	A17	CPU_DATA<48>	6 8 36
D_49	B17	CPU_DATA<49>	6 8 36
D_50	E18	CPU_DATA<50>	6 8 36
D_51	B18	CPU_DATA<51>	6 8 36
D_52	D18	CPU_DATA<52>	6 8 36
D_53	A18	CPU_DATA<53>	6 8 36
D_54	A19	CPU_DATA<54>	6 8 36
D_55	H19	CPU_DATA<55>	6 8 36
D_56	B19	CPU_DATA<56>	6 8 36
D_57	J19	CPU_DATA<57>	6 8 36
D_58	A20	CPU_DATA<58>	6 8 36
D_59	D19	CPU_DATA<59>	6 8 36
D_60	E19	CPU_DATA<60>	6 8 36
D_61	G19	CPU_DATA<61>	6 8 36
D_62	B20	CPU_DATA<62>	6 8 36
D_63	G20	CPU_DATA<63>	6 8 36
DBG	A30	CPU_DBG_L	5 8 36
DRDY	G28	CPU_DRDY_L	5 8 36
DTI_0	K25	CPU_DTI<0>	5 36
DTI_1	D29	CPU_DTI<1>	5 36
DTI_2	B30	CPU_DTI<2>	5 36
TA	E27	CPU_TA_L	5 8 36
TEA	E28	CPU_TEA_L	5 8 36

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R169 511 1% 1/16W MF 402
R168 0 5% 1/16W MF 402
R161 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT	R155 0	INT_CPUFB_OUT_SHORT	R140 0	
INT_CPUFB_OUT_NORM	R128 0	INT_CPUFB_LONG		
INT_CPUFB_IN	R146[1] 0	R147 0	R141[1] 0	R136 0
INT_CPUFB_IN_NORM				

All: 5% 1/16W MF 402

MAXBUS PULL-UPS

MAXBUS_SLEEP

RP3 10K	CPU_TS_L	RP3 10K	CPU_TA_L	RP3 10K	CPU_ARTRY_L	RP2 10K	CPU_BR_L
R152 10K	CPU_HIT_L	RP2 10K	CPU_DRDY_L	RP2 10K	CPU_TEA_L	RP2 10K	CPU_AACK_L
R150 10K	CPU_DBG_L	RP3 10K	CPU_BG_L	R151 10K	CPU_QREQ_L		

All: 5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF R669[1] 10K	NO STUFF R645[1] 10K	NO STUFF R697[1] 10K	NO STUFF R670[1] 10K	R644[1] 10K	NO STUFF R646[1] 10K		
CPU_DATA<56>	CPU_DATA<57>	CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>

R656[1] 10K	R685[1] 10K	R657[1] 10K	R628[1] 10K	R682[1] 10K	R658[1] 10K	NO STUFF R627[1] 10K	R629[1] 10K
Spare	Spare	OBSOLETE ROM Only, Req PCI1 0: 1 IDE 1: 0 1 IDE 2 2:3 PCI1	0: Disable PCI1_REQ2_L / PCI1_GNT2_L 1: GPIO2	0: Disable PCI1_REQ1_L / PCI1_GNT1_L 1: GPIO1	0: Disable PCI1_REQ0_L / PCI1_GNT0_L 1: GPIO0	Firewire PHY interface 0: B-Mode interface	Processor Bus Mode 0: 60x Bus (G3) 1: 60x Bus (G4)

All: 5% 1/16W MF 402

Intrepid MaxBus	

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SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U51
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	MEM_DATA<0>	10
DDR_DATA_1	AK33	MEM_DATA<1>	10
DDR_DATA_2	AK31	MEM_DATA<2>	10
DDR_DATA_3	AK35	MEM_DATA<3>	10
DDR_DATA_4	AK36	MEM_DATA<4>	10
DDR_DATA_5	AJ32	MEM_DATA<5>	10
DDR_DATA_6	AJ35	MEM_DATA<6>	10
DDR_DATA_7	AJ36	MEM_DATA<7>	10
DDR_DATA_8	AG33	MEM_DATA<8>	10
DDR_DATA_9	AG35	MEM_DATA<9>	10
DDR_DATA_10	AH35	MEM_DATA<10>	10
DDR_DATA_11	AG36	MEM_DATA<11>	10
DDR_DATA_12	AH36	MEM_DATA<12>	10
DDR_DATA_13	AH32	MEM_DATA<13>	10
DDR_DATA_14	AG32	MEM_DATA<14>	10
DDR_DATA_15	AG31	MEM_DATA<15>	10
DDR_DATA_16	AE32	MEM_DATA<16>	10
DDR_DATA_17	AF35	MEM_DATA<17>	10
DDR_DATA_18	AF36	MEM_DATA<18>	10
DDR_DATA_19	AE36	MEM_DATA<19>	10
DDR_DATA_20	AE35	MEM_DATA<20>	10
DDR_DATA_21	AE33	MEM_DATA<21>	10
DDR_DATA_22	AD36	MEM_DATA<22>	10
DDR_DATA_23	AD35	MEM_DATA<23>	10
DDR_DATA_24	AA36	MEM_DATA<24>	10
DDR_DATA_25	AA35	MEM_DATA<25>	10
DDR_DATA_26	AA33	MEM_DATA<26>	10
DDR_DATA_27	AB36	MEM_DATA<27>	10
DDR_DATA_28	AB35	MEM_DATA<28>	10
DDR_DATA_29	AC36	MEM_DATA<29>	10
DDR_DATA_30	AA32	MEM_DATA<30>	10
DDR_DATA_31	AB33	MEM_DATA<31>	10
DDR_DATA_32	V36	MEM_DATA<32>	10
DDR_DATA_33	U33	MEM_DATA<33>	10
DDR_DATA_34	U32	MEM_DATA<34>	10
DDR_DATA_35	V35	MEM_DATA<35>	10
DDR_DATA_36	T36	MEM_DATA<36>	10
DDR_DATA_37	U36	MEM_DATA<37>	10
DDR_DATA_38	U35	MEM_DATA<38>	10
DDR_DATA_39	T36	MEM_DATA<39>	10
DDR_DATA_40	P33	MEM_DATA<40>	10
DDR_DATA_41	R36	MEM_DATA<41>	10
DDR_DATA_42	P35	MEM_DATA<42>	10
DDR_DATA_43	P36	MEM_DATA<43>	10
DDR_DATA_44	R36	MEM_DATA<44>	10
DDR_DATA_45	R35	MEM_DATA<45>	10
DDR_DATA_46	R33	MEM_DATA<46>	10
DDR_DATA_47	R32	MEM_DATA<47>	10
DDR_DATA_48	N35	MEM_DATA<48>	10
DDR_DATA_49	M36	MEM_DATA<49>	10
DDR_DATA_50	L35	MEM_DATA<50>	10
DDR_DATA_51	M35	MEM_DATA<51>	10
DDR_DATA_52	M33	MEM_DATA<52>	10
DDR_DATA_53	L36	MEM_DATA<53>	10
DDR_DATA_54	N33	MEM_DATA<54>	10
DDR_DATA_55	M36	MEM_DATA<55>	10
DDR_DATA_56	J32	MEM_DATA<56>	10
DDR_DATA_57	J33	MEM_DATA<57>	10
DDR_DATA_58	J35	MEM_DATA<58>	10
DDR_DATA_59	K32	MEM_DATA<59>	10
DDR_DATA_60	K33	MEM_DATA<60>	10
DDR_DATA_61	J36	MEM_DATA<61>	10
DDR_DATA_62	K36	MEM_DATA<62>	10
DDR_DATA_63	K35	MEM_DATA<63>	10

DDR_A_0	H35	MEM_ADDR<0>	9 35
DDR_A_1	G35	MEM_ADDR<1>	9 35
DDR_A_2	G36	MEM_ADDR<2>	9 35
DDR_A_3	F36	MEM_ADDR<3>	9 35
DDR_A_4	F35	MEM_ADDR<4>	9 35
DDR_A_5	E35	MEM_ADDR<5>	9 35
DDR_A_6	E36	MEM_ADDR<6>	9 35
DDR_A_7	G32	MEM_ADDR<7>	9 35
DDR_A_8	D36	MEM_ADDR<8>	9 35
DDR_A_9	H36	MEM_ADDR<9>	9 35
DDR_A_10	G33	MEM_ADDR<10>	9 35
DDR_A_11	H33	MEM_ADDR<11>	9 35
DDR_A_12	D35	MEM_ADDR<12>	9 35
DDR_BA_0	L30	MEM_BA<0>	9 35
DDR_BA_1	M29	MEM_BA<1>	9 35
DDRCS_0	AN34	MEM_CS_L<0>	9 35
DDRCS_1	AN36	MEM_CS_L<1>	9 35
DDRCS_2	AL35	MEM_CS_L<2>	9 35
DDRCS_3	AL33	MEM_CS_L<3>	9 35
DDR_DQS_0	AJ31	MEM_DQS<0>	10 35
DDR_DQS_1	AH31	MEM_DQS<1>	10 35
DDR_DQS_2	AD32	MEM_DQS<2>	10 35
DDR_DQS_3	AB30	MEM_DQS<3>	10 35
DDR_DQS_4	V30	MEM_DQS<4>	10 35
DDR_DQS_5	P32	MEM_DQS<5>	10 35
DDR_DQS_6	N29	MEM_DQS<6>	10 35
DDR_DQS_7	L32	MEM_DQS<7>	10 35
DDR_DM_0	AJ33	MEM_DQM<0>	10 35
DDR_DM_1	AH33	MEM_DQM<1>	10 35
DDR_DM_2	AD33	MEM_DQM<2>	10 35
DDR_DM_3	AC35	MEM_DQM<3>	10 35
DDR_DM_4	T35	MEM_DQM<4>	10 35
DDR_DM_5	T33	MEM_DQM<5>	10 35
DDR_DM_6	N32	MEM_DQM<6>	10 35
DDR_DM_7	L33	MEM_DQM<7>	10 35
DDRRAS	L29	MEM_RAS_L	9 35
DDRCAS	H32	MEM_CAS_L	9 35
DDRWE	K30	MEM_WE_L	9 35
DDRCKE0	AN35	MEM_CKE<0>	9 35
DDRCKE1	AM35	MEM_CKE<1>	9 35
DDRCKE2	AM36	MEM_CKE<2>	9 35
DDRCKE3	AL36	MEM_CKE<3>	9 35
DDR_SELHI_0	AB32	MEM_MUXSEL_MSB_L_TP	
DDR_SELHI_1	AE29	MEM_MUXSEL_MSB	10 35
DDR_SELLO_0	N30	MEM_MUXSEL_LSB_L_TP	
DDR_SELLO_1	T32	MEM_MUXSEL_LSB	10 35
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 35
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 35
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 35
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 35
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 35
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 35
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 35
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 35
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF_H	38
DDR_VREF_0	Y22	INT_MEM_VREF	9 38
DDR_VREF_1	T22		

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

MEM_VREF

R209 1K 1% 1/16W MF 402

+2_5V_INTREPID

R208 10K 1% 1/16W MF 402

R202 10K 1% 1/16W MF 402

C249 0.1uF 20% 10V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP20	4	5	SYSCLK_DDRCLK_A1	11 35
SYSCLK_DDRCLK_A1_L_UF	RP20	3	6	SYSCLK_DDRCLK_A1_L	11 35
SYSCLK_DDRCLK_A0_UF	RP22	1	8	SYSCLK_DDRCLK_A0	11 35
SYSCLK_DDRCLK_A0_L_UF	RP22	2	7	SYSCLK_DDRCLK_A0_L	11 35
SYSCLK_DDRCLK_B1_UF	RP20	2	7	SYSCLK_DDRCLK_B1	11 35
SYSCLK_DDRCLK_B1_L_UF	RP20	1	8	SYSCLK_DDRCLK_B1_L	11 35
SYSCLK_DDRCLK_B0_UF	RP22	3	6	SYSCLK_DDRCLK_B0	11 35
SYSCLK_DDRCLK_B0_L_UF	RP22	4	5	SYSCLK_DDRCLK_B0_L	11 35

CS

MEM_CS_L<0>	RP31	3	6	RAM_CS_L<0>	11 35
MEM_CS_L<1>	RP31	2	7	RAM_CS_L<1>	11 35
MEM_CS_L<2>	RP29	3	6	RAM_CS_L<2>	11 35
MEM_CS_L<3>	RP29	4	5	RAM_CS_L<3>	11 35

CKE

MEM_CKE<0>	RP31	1	8	RAM_CKE<0>	9 11 35
MEM_CKE<1>	RP31	4	5	RAM_CKE<1>	9 11 35
MEM_CKE<2>	RP29	1	8	RAM_CKE<2>	9 11 35
MEM_CKE<3>	RP29	2	7	RAM_CKE<3>	9 11 35

ADDR

MEM_ADDR<0>	RP14	3	6	RAM_ADDR<0>	11 35
MEM_ADDR<1>	RP12	2	7	RAM_ADDR<1>	11 35
MEM_ADDR<2>	RP12	1	8	RAM_ADDR<2>	11 35
MEM_ADDR<3>	RP12	4	5	RAM_ADDR<3>	11 35
MEM_ADDR<4>	RP12	3	6	RAM_ADDR<4>	11 35
MEM_ADDR<5>	RP9	2	7	RAM_ADDR<5>	11 35
MEM_ADDR<6>	RP9	1	8	RAM_ADDR<6>	11 35
MEM_ADDR<7>	RP14	2	7	RAM_ADDR<7>	11 35
MEM_ADDR<8>	RP9	4	5	RAM_ADDR<8>	11 35
MEM_ADDR<9>	RP14	4	5	RAM_ADDR<9>	11 35
MEM_ADDR<10>	RP14	1	8	RAM_ADDR<10>	11 35
MEM_ADDR<11>	RP17	4	5	RAM_ADDR<11>	11 35
MEM_ADDR<12>	RP9	3	6	RAM_ADDR<12>	11 35

BA

MEM_BA<0>	RP17	2	7	RAM_BA<0>	11 35
MEM_BA<1>	RP17	1	8	RAM_BA<1>	11 35

CNTL

MEM_WE_L	RP17	3	6	RAM_WE_L	11 35
MEM_CAS_L	R162	1	2	RAM_CAS_L	11 35
MEM_RAS_L	R176	1	2	RAM_RAS_L	11 35

1MB BOOT ROM

+3V_MAIN

C125 2.2uF 20% 10V CERM 805

C773 0.1uF 20% 10V CERM 402

C122 0.1uF 20% 10V CERM 402

U11
FEPR-1MX8
110
TSOP

VPP 11
VCC 30, 31

A0	21	DQ0	25
A1	20	DQ1	26
A2	19	DQ2	27
A3	18	DQ3	28
A4	17	DQ4	32
A5	16	DQ5	33
A6	15	DQ6	34
A7	14	DQ7	35
A8	8		
A9	7		
A10	36		
A11	6		
A12	5		
A13	4		
A14	3		
A15	2		
A16	1		
A17	40		
A18	13		
A19	37		
A20	38		
CE	22		
OE	24		
WE	9		
WP	12		
PWD	10		
GND	23, 39		

DQ0	25	PCI_AD<24>
DQ1	26	PCI_AD<25>
DQ2	27	PCI_AD<26>
DQ3	28	PCI_AD<27>
DQ4	32	PCI_AD<28>
DQ5	33	PCI_AD<29>
DQ6	34	PCI_AD<30>
DQ7	35	PCI_AD<31>

A0	21	PCI_AD<0>
A1	20	PCI_AD<1>
A2	19	PCI_AD<2>
A3	18	PCI_AD<3>
A4	17	PCI_AD<4>
A5	16	PCI_AD<5>
A6	15	PCI_AD<6>
A7	14	PCI_AD<7>
A8	8	PCI_AD<8>
A9	7	PCI_AD<9>
A10	36	PCI_AD<10>
A11	6	PCI_AD<11>
A12	5	PCI_AD<12>
A13	4	PCI_AD<13>
A14	3	PCI_AD<14>
A15	2	PCI_AD<15>
A16	1	PCI_AD<16>
A17	40	PCI_AD<17>
A18	13	PCI_AD<18>
A19	37	PCI_AD<19>
A20	38	PCI_AD<20>

+3V_MAIN

R691 10K 5% 1/16W MF 402

R112 10K 5% 1/16W MF 402

R674 1K 5% 1/16W MF 402

ROM_CS_L

ROM_ONBOARD_CS_L
ROM_OE_L
ROM_RW_L
ROM_WP_L
INT_RESET_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0104	335S0350		U11	Alt for Sharp BootRom

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

R247 10K 5% 1/16W MF 402 — INT_2_5V_COLD

R257 10K 5% 1/16W MF 402 — INT_2_5V_COLD

R260 10K 5% 1/16W MF 402 — INT_2_5V_COLD

R265 10K 5% 1/16W MF 402 — INT_2_5V_COLD

INT - DDR/BOOTROM

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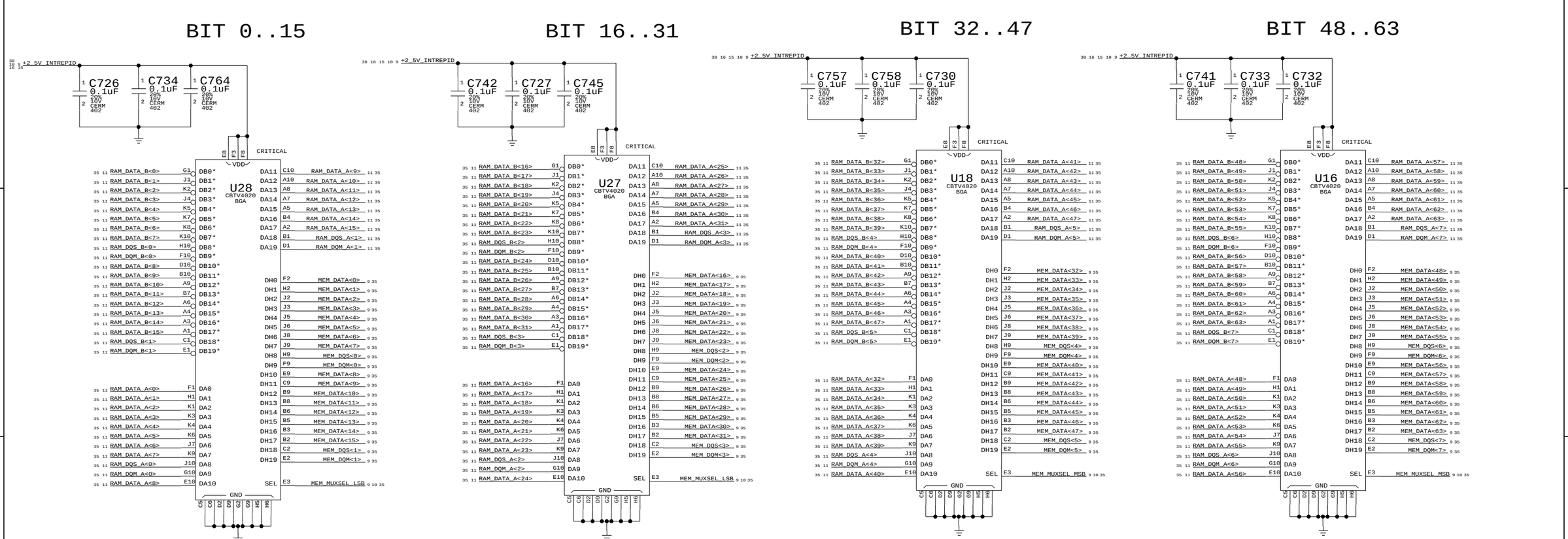
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SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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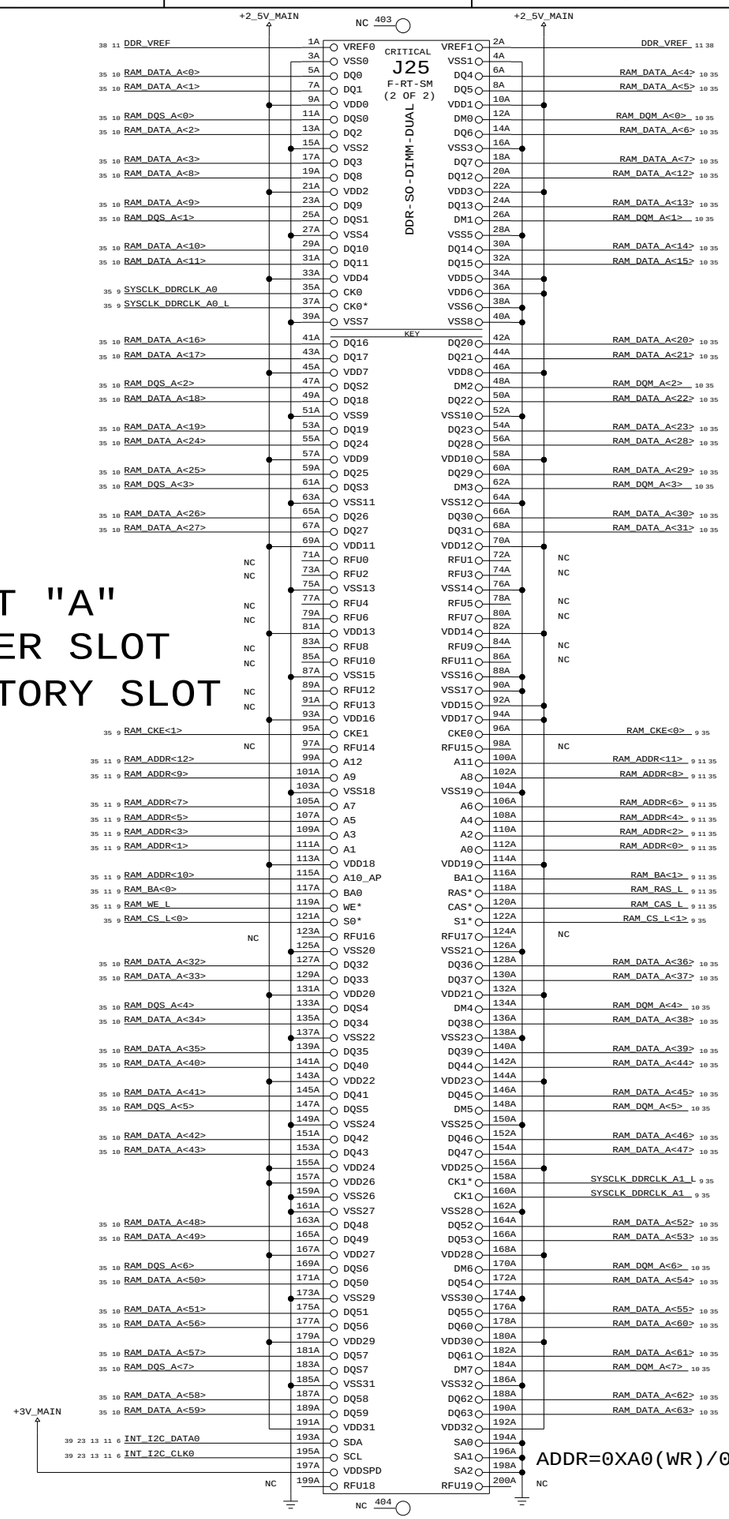
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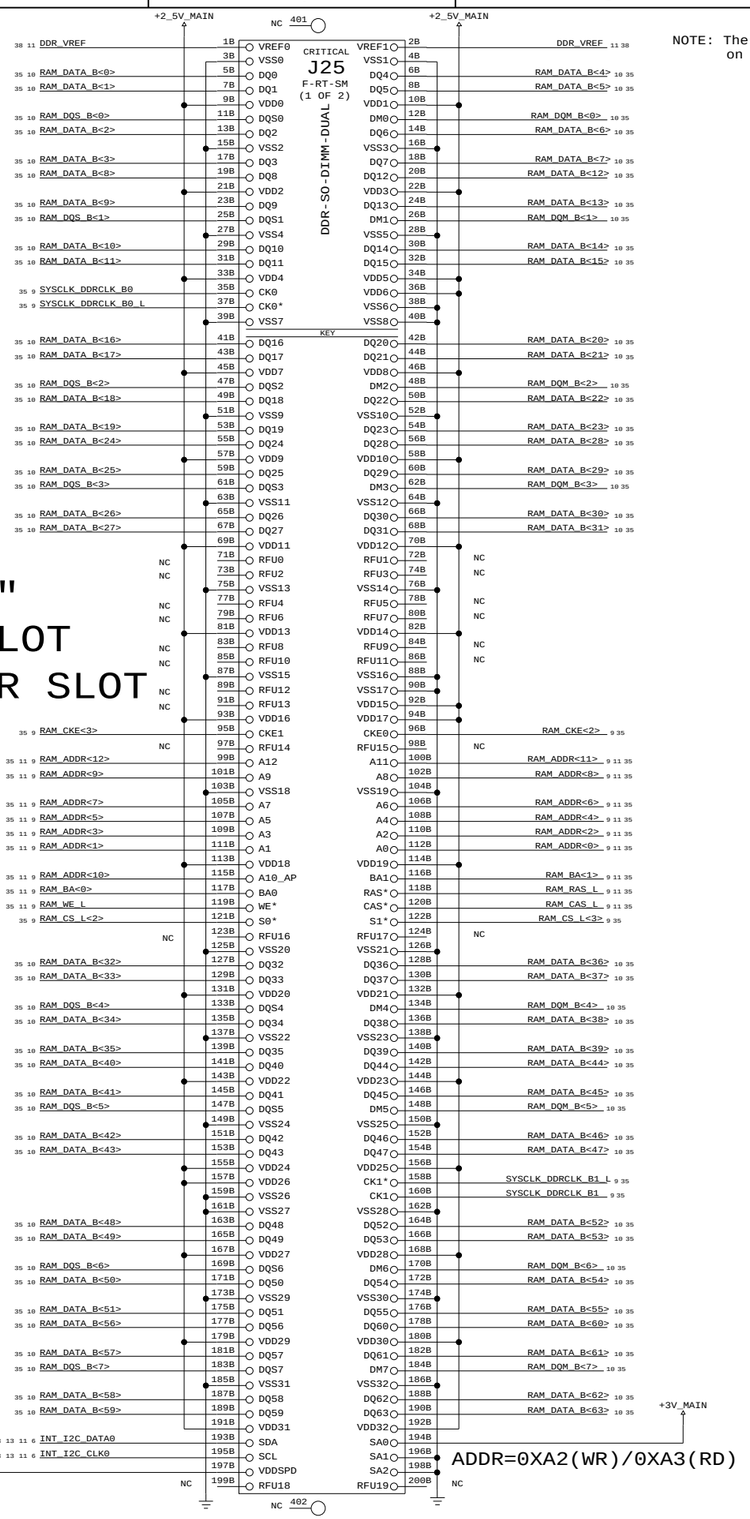
SIZE	DRAWING NUMBER	REV.
D	401243	0A

SCALE	SHT
NONE	10 OF 44

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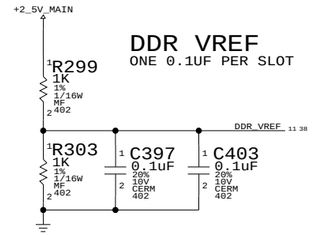


SLOT "A"
LOWER SLOT
FACTORY SLOT



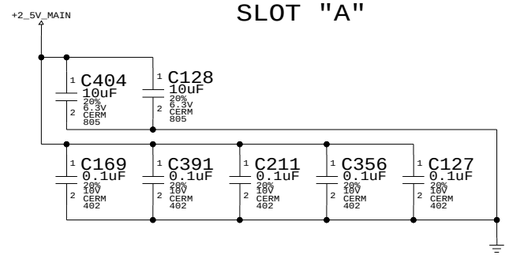
SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting

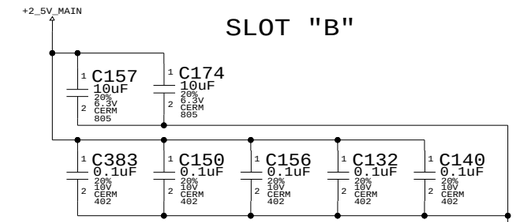


DDR VREF
ONE 0.1UF PER SLOT

DDR BYPASS
SLOT "A"



SLOT "B"



DDR SODIMM CONNS

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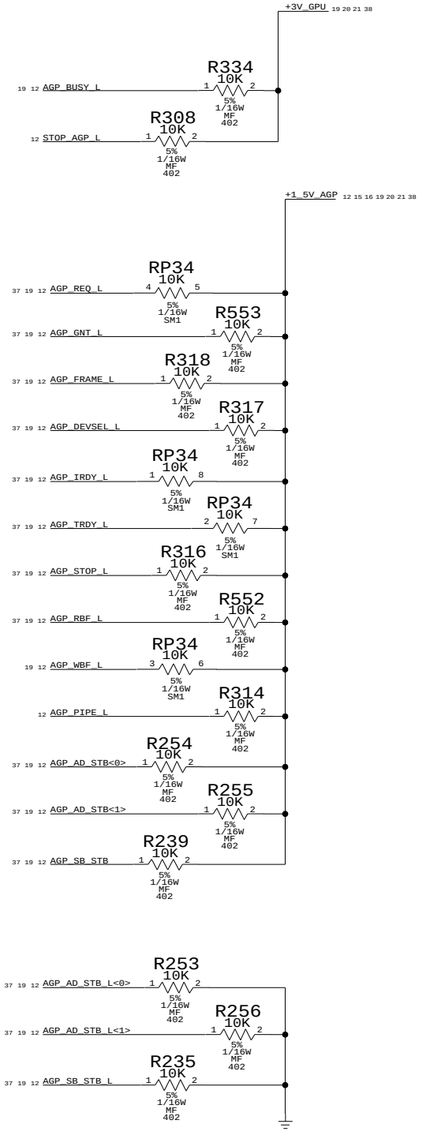
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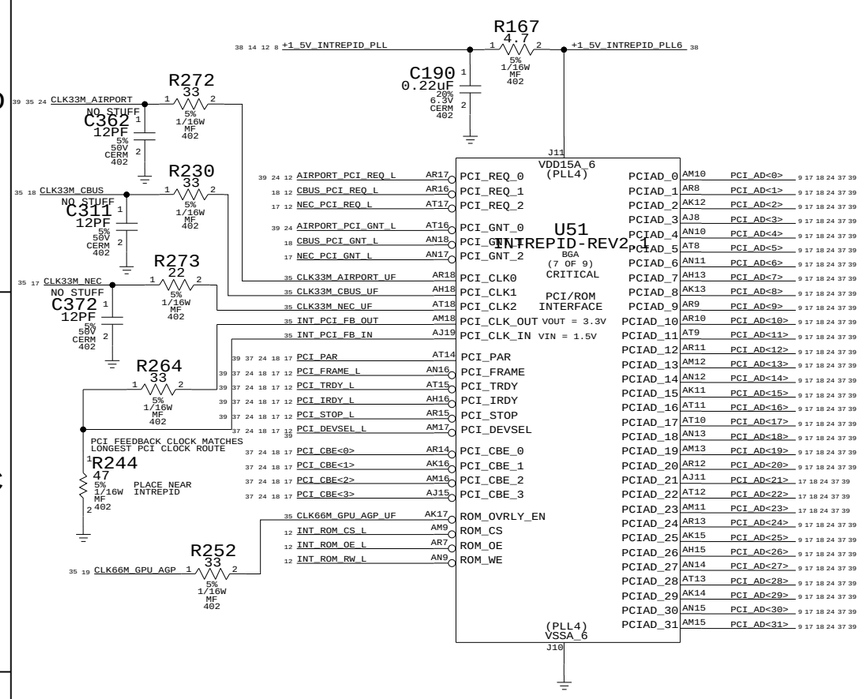
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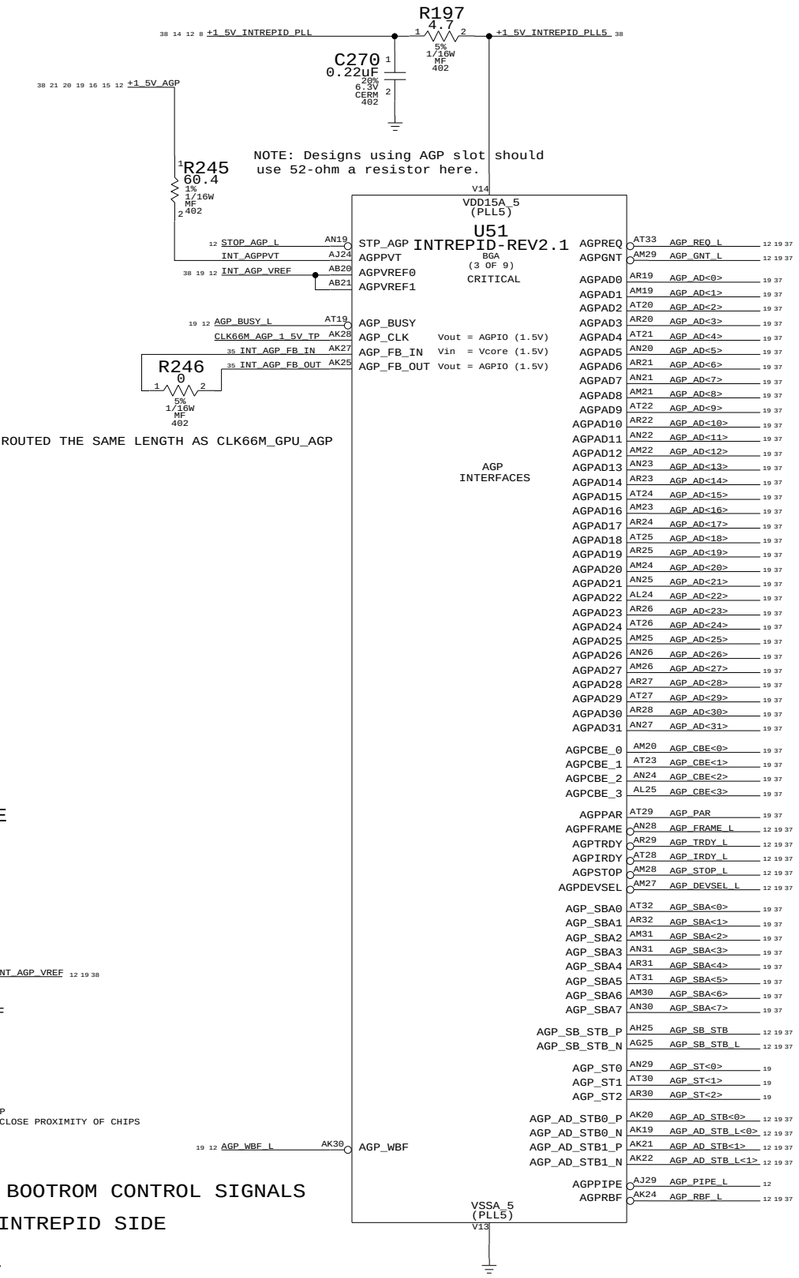
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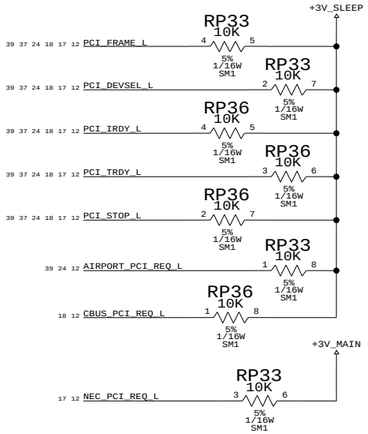
AGP PULL-UPS/PULL DOWNS







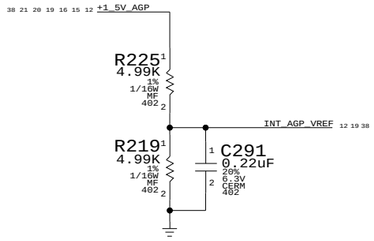
PCI PULL-UPS



NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP

AGP I/O REFERENCE

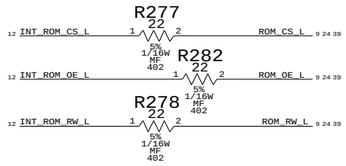
(PLACE CLOSE TO INTREPID AGP BALLS)



SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

PLACE CLOSE TO INTREPID SIDE



INTREPID AGP/PCI

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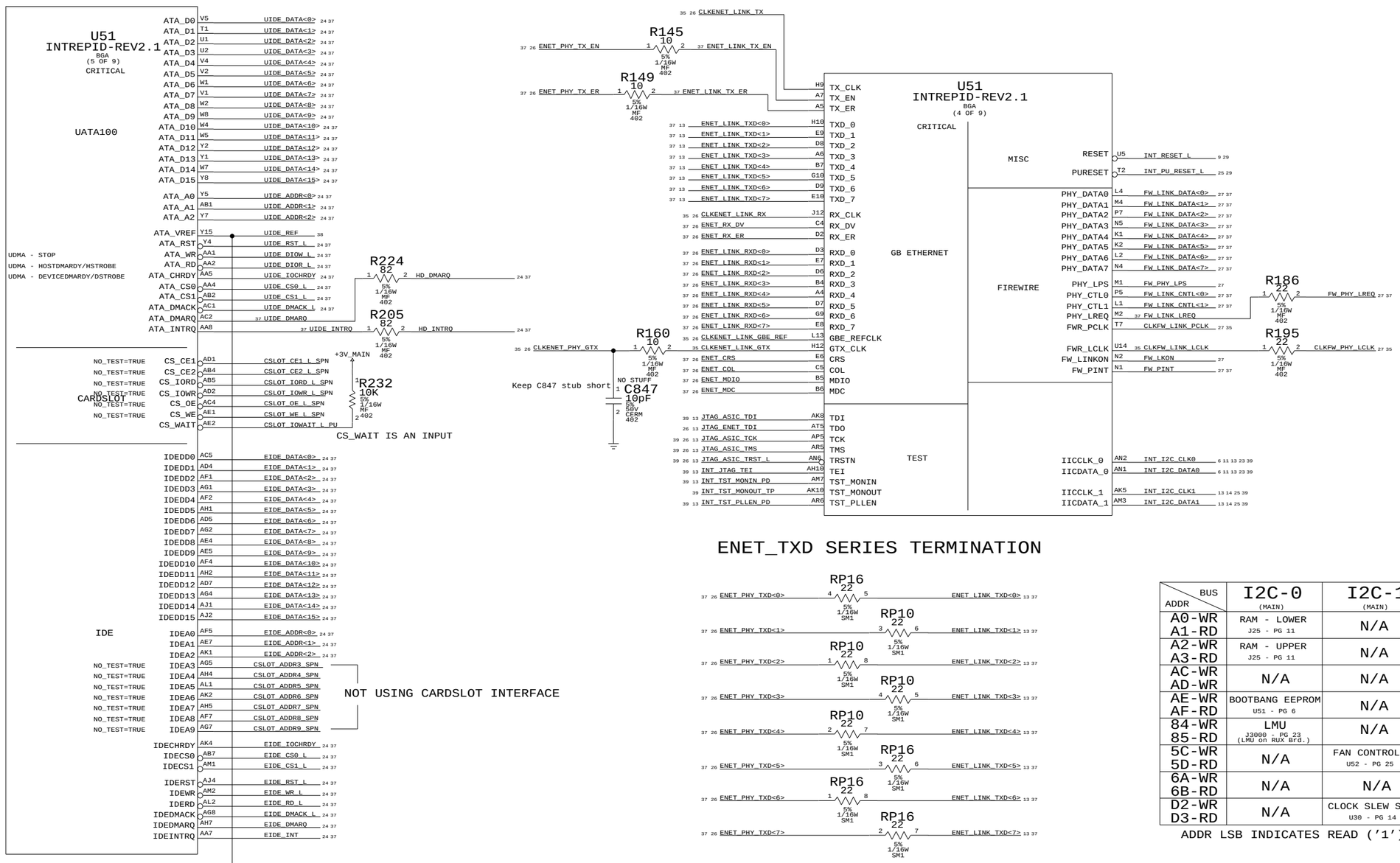
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BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K — USB_DAM
R183 10K — USB_DAP
R156 10K — USB_DBM
R157 10K — USB_DBP
R164 10K — USB_DCM
R165 10K — USB_DCP
R182 10K — USB_DDM
R180 10K — USB_DDP

PORT E/BLUETOOTH

R174 22 — USB_DEP ↔ BT_USB_DP
R179 22 — USB_DEM ↔ BT_USB_DM
R178 15K — BT_USB_DP
R175 15K — BT_USB_DM

PORT F/MODEM

R192 22 — USB_DFP ↔ MODEM_USB_DP
R188 22 — USB_DFM ↔ MODEM_USB_DM
R189 15K — MODEM_USB_DP
R193 15K — MODEM_USB_DM

PCI INTERRUPTS

R148 10K — CBUS_INT_L
R746 10K — AIRPORT_PCI_INT_L
R158 10K — NEC_PCI_INT_L

GPIO/EXTINT PULLUPS

R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP5 10K — INT_EXTINT11_PU
RP6 10K — INT_EXTINT10_PU
RP4 10K — INT_EXTINT12_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K (USB MODEM) — INT_MOD_DTO_UF
RP15 10K (USB MODEM) — INT_MOD_CLKOUT_UF
RP15 10K (USB MODEM) — INT_MOD_DTI
RP15 10K (USB MODEM) — INT_MOD_SYNC_UF
R206 10K (USB MODEM) — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

U49 LT1962-ADJ MSOP: IN ← LTC1962_INT_VIN; OUT → +1_5V_INTREPID_PLL → -> 1.55V OUTPUT; ADJ ← LT1962_INT_ADJ; BYP ← LT1962_INT_BYP; SHDN ← +3V_SLEEP; NC
C721 1uF 10V CERM 603
C392 0.01uF 10V CERM 402
R574 18.7K 1% 1/16W MF 402
R567 68.1K 1% 1/16W MF 402
C723 10uF 6.3V CERM 805

R240 4.7 — +1_5V_INTREPID_PLL8
R280 4.7 — +1_5V_INTREPID_PLL4
R279 4.7 — +1_5V_INTREPID_PLL3
R243 4.7 — +1_5V_INTREPID_PLL2
R201 4.7 — +1_5V_INTREPID_PLL1
C337 0.22uF 6.3V CERM 402
C389 0.22uF 6.3V CERM 402
C388 0.22uF 6.3V CERM 402
C386 0.22uF 6.3V CERM 402
C387 0.22uF 6.3V CERM 402

L13 FERR-EMI-100-OHM SM — +3V_MAIN
C235 0.01uF 16V CERM 402
C246 0.1uF 10V CERM 402
C256 10uF 6.3V CERM 805
+3V_INTREPID_USB

L15 400-OHM-EMI SM-1 — +3V_MAIN
L14 400-OHM-EMI SM-1 — +2_5V_MAIN
C400 0.1uF 10V CERM 402
C402 1uF 10V CERM 603
C399 0.1uF 10V CERM 402
C394 0.1uF 10V CERM 402
+3V_CG_PLL_MAIN
+2_5V_CG_MAIN
MAIN_RESET_L
R286 0 — NO STUFF
R287 10K
R288 10K
R295 10K — NO STUFF

U51 INTRENPID-REV2.1 CRITICAL BGA (6 OF 9)

GPIO: GPIO0 (VCORE A/B SEL), GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO9, GPIO11, GPIO12, GPIO15, GPIO16 — GENERAL PURPOSE I/O'S
INTERRUPTS: EXTINT0, EXTINT1, EXTINT2, EXTINT3, EXTINT4, EXTINT5, EXTINT6, EXTINT7, EXTINT8 (POWERBOOK SPARE), EXTINT9, EXTINT10 (CBUS_REG_L), EXTINT11 (CBUS_IREQ_L), EXTINT12, EXTINT13, EXTINT14, EXTINT15, EXTINT16, EXTINT17, CPU_INT, PCIPME, PROCSLEEPREQ, PENDPROCINT
CLOCKS: XTAL_IN, XTAL_OUT, STOPXTAL, WATCHDOG, BUF_REF_CLK_OUT, SS_REF_CLK_IN
USB: SCCTXDA, SCCRTSA, SCCDTRA, SCCRXDA, SCCGPIOA, SCCTRXCA, SCCTXDB, SCCRTSB, SCCRXDB, SCCGPIOB, SCCTRXCB, USB_VD0_P/N, USB_VD1_P/N, USB_VD2_P/N, USB_VD3_P/N, USB_PRTPWR0, USB_PWRFLT0, USB_PRTPWR1, USB_PWRFLT1, USB_PRTPWR2, USB_PWRFLT2
AUDIO/I2S: AUD_DTO, AUD_DTI, AUD_SYNC, AUD_BITCLK, AUD_CLKOUT, MOD_DTO, MOD_DTI (SIGNAL FROM MODEM), MOD_SYNC, MOD_BITCLK, MOD_CLKOUT
IIC: IICCLK_2, IICDATA_2
PCI VDD15A_1 (PLL1), VDD15A_2 (PLL2), VDD15A_3 (PLL3), VDD15A_4 (PLL7), VDD15A_8 (PLL9)
VDDU33_1, VDDU33_2
VSSA1 (PLL1), VSSA2 (PLL2), VSSA3 (PLL3), VSSA4 (PLL7), VSSA_8 (PLL9), VSSU_1, VSSU_2

U31 CY28512D TSSOP SSCG — INTERNAL 250K PULL-UP; OUTPUT IMPEDANCE ~18-20 OHMS
CLKIN, FSEL, SCLK, SDATA, ADDRSEL INTERNAL 250K PULL-DOWN, RESET*, PD*, LOCK OPEN DRAIN OUTPUT, ODSEL INTERNAL 250K PULL-UP
CPU0, VDDQ1, VDDQ10, VDDQ12, VDDQ5, VDDQ18, VSS0, VSS1, VSSA, VSSC, VSSQ
R293 33 — INT_REF_CLK_IN
R292 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
R142 0 — VCORE_VGATE
R284 0 — VCORE_VGATE
R296 10K

J9 U.FL-R_SMT F-ST-SM — CLK18M_INT_EXT
R134 0 — NO STUFF
R113 51 — NO STUFF
R144 10M — NO STUFF
R143 0
Y2 18.432M SM — CRITICAL — CLK18M_XTAL_IN
C152 22pF — CRYSTAL LOAD CAPACITANCE IS 16PF
C151 22pF
R218 0 — INT_REF_CLK_OUT

HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

R258 1K — INT_I2C_CLK2
R241 1K — INT_I2C_DATA2
+3V_SLEEP

RP13 47 — INT_I2S0_SND_TO_DAC
RP13 47 — INT_I2S0_SND_LRCLK
RP13 47 — INT_I2S0_SND_SCLK
RP13 47 — INT_I2S0_SND_MCLK
SOFT_MODEM RP47 47 — INT_MOD_DTO
SOFT_MODEM RP47 47 — INT_MOD_SYNC
SOFT_MODEM RP47 47 — INT_MOD_BITCLK
SOFT_MODEM RP47 47 — INT_MOD_CLKOUT

INT - USB/GPIOS/I2S

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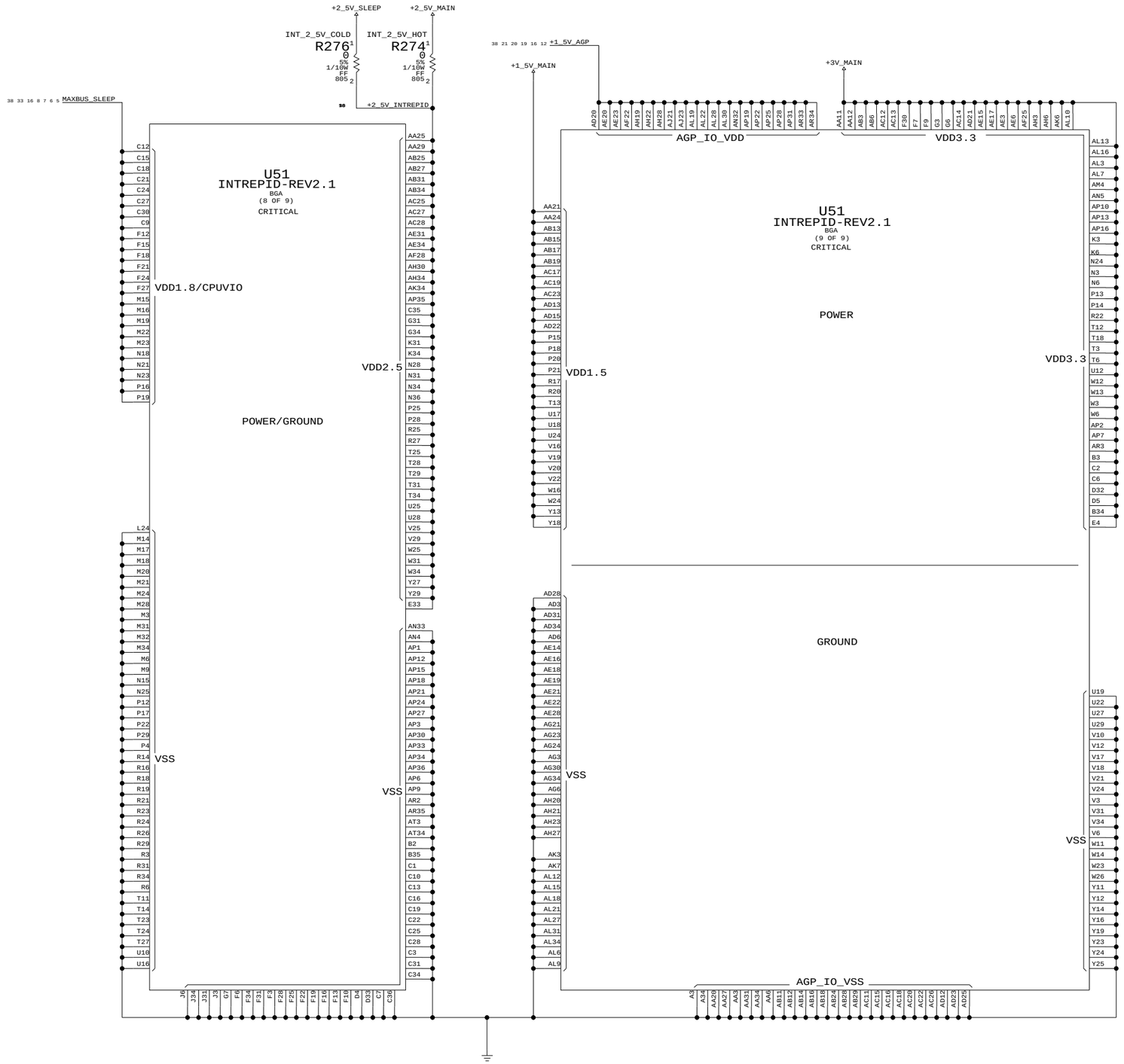
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PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

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Intrepid Power

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INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

33 15 8 7 6 5 MAXBUS_SLEEP

C148 10uF 20% 6.3V CERM 805 · C142 10uF 20% 6.3V CERM 805 · C144 10uF 20% 6.3V CERM 805 · C146 10uF 20% 6.3V CERM 805

C182 0.22uF · C178 0.22uF · C141 0.22uF · C145 0.22uF · C214 0.22uF · C163 0.22uF · C164 0.22uF · C225 0.22uF · C160 0.22uF · C159 0.22uF
C204 0.22uF · C166 0.22uF · C205 0.22uF · C223 0.22uF · C229 0.22uF · C181 0.22uF · C207 0.22uF · C208 0.22uF · C183 0.22uF · C180 0.22uF
C165 0.22uF · C206 0.22uF · C147 0.22uF · C149 0.22uF · C179 0.22uF · C162 0.22uF · C161 0.22uF · C213 0.22uF

(20% 6.3V CERM 402)

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF 20% 6.3V CERM 805 · C325 10uF 20% 6.3V CERM 805 · C201 10uF 20% 6.3V CERM 805 · C200 10uF 20% 6.3V CERM 805

C299 0.22uF · C279 0.22uF · C262 0.22uF · C292 0.22uF · C248 0.22uF · C302 0.22uF · C300 0.22uF · C290 0.22uF · C272 0.22uF · C259 0.22uF
C301 0.22uF · C278 0.22uF · C226 0.22uF · C238 0.22uF · C250 0.22uF · C263 0.22uF · C224 0.22uF · C222 0.22uF · C261 0.22uF · C227 0.22uF
C271 0.22uF · C310 0.22uF · C288 0.22uF · C260 0.22uF · C303 0.22uF · C287 0.22uF · C258 0.22uF · C236 0.22uF · C289 0.22uF

(20% 6.3V CERM 402)

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

38 21 20 19 15 12 +1_5V_AGP

C381 10uF 20% 6.3V CERM 805 · C380 10uF 20% 6.3V CERM 805 · C382 10uF 20% 6.3V CERM 805 · C379 10uF 20% 6.3V CERM 805

C367 0.22uF · C319 0.22uF · C330 0.22uF · C363 0.22uF · C366 0.22uF · C332 0.22uF · C361 0.22uF · C320 0.22uF · C328 0.22uF · C364 0.22uF
C365 0.22uF · C329 0.22uF · C345 0.22uF · C346 0.22uF · C373 0.22uF · C344 0.22uF · C331 0.22uF · C312 0.22uF · C354 0.22uF · C347 0.22uF
C321 0.22uF

(20% 6.3V CERM 402)

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF 20% 6.3V CERM 805 · C376 10uF 20% 6.3V CERM 805 · C377 10uF 20% 6.3V CERM 805 · C375 10uF 20% 6.3V CERM 805

C170 0.22uF · C358 0.22uF · C268 0.22uF · C327 0.22uF · C342 0.22uF · C215 0.22uF · C352 0.22uF · C171 0.22uF · C158 0.22uF · C309 0.22uF
C175 0.22uF · C357 0.22uF · C351 0.22uF · C350 0.22uF · C286 0.22uF · C176 0.22uF · C189 0.22uF · C167 0.22uF · C371 0.22uF · C359 0.22uF
C285 0.22uF · C283 0.22uF · C269 0.22uF · C221 0.22uF · C234 0.22uF · C247 0.22uF · C257 0.22uF · C343 0.22uF · C313 0.22uF · C228 0.22uF
C360 0.22uF · C308 0.22uF · C318 0.22uF · C237 0.22uF · C317 0.22uF · C341 0.22uF · C177 0.22uF · C212 0.22uF · C349 0.22uF · C184 0.22uF

(20% 6.3V CERM 402)

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C314 10uF 20% 6.3V CERM 805 · C322 10uF 20% 6.3V CERM 805 · C191 10uF 20% 6.3V CERM 805 · C202 10uF 20% 6.3V CERM 805

C304 0.22uF · C266 0.22uF · C172 0.22uF · C281 0.22uF · C243 0.22uF · C253 0.22uF · C334 0.22uF · C241 0.22uF · C348 0.22uF · C192 0.22uF
C306 0.22uF · C252 0.22uF · C275 0.22uF · C297 0.22uF · C240 0.22uF · C218 0.22uF · C274 0.22uF · C369 0.22uF · C368 0.22uF · C168 0.22uF
C265 0.22uF · C251 0.22uF · C216 0.22uF · C254 0.22uF · C305 0.22uF · C186 0.22uF · C219 0.22uF · C315 0.22uF · C264 0.22uF · C294 0.22uF
C323 0.22uF · C273 0.22uF · C242 0.22uF · C203 0.22uF · C333 0.22uF · C217 0.22uF · C230 0.22uF · C293 0.22uF · C231 0.22uF · C296 0.22uF
C239 0.22uF · C316 0.22uF · C185 0.22uF · C282 0.22uF · C295 0.22uF · C280 0.22uF

(20% 6.3V CERM 402)

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF · C139 0.22uF · C335 0.22uF · C735 0.22uF · C245 0.22uF · C736 0.22uF · C739 0.22uF · C395 0.22uF · C374 0.22uF · C385 0.22uF

(20% 6.3V CERM 402)

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

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SIZE	DRAWING NUMBER	REV.
D	401243	0A

SCALE	SHT
NONE	16 OF 44

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C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402
+3V_NEC_VDD 17 38

+3V_MAIN
L7 FERR-EMI-100-OHM SM
R172 0 5% 1/16W MF 603
C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805
38 NEC_AVDD
38 17 +3V_NEC_VDD

Y1's LOAD CAPACITANCE = 16 pF
CRITICAL
Y1 30.0000M SM-1
NEC_XT2_R
C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

R613 36 1% 1/16W MF 402 — NEC_USB_DAM 25 37 39
Low/Full/High Speed (External)
R612 36 1% 1/16W MF 402 — NEC_USB_DAP 25 37 39
R609 36 1% 1/16W MF 402 — NEC_USB_DBM 25 37 39
Low/Full/High Speed (External)
R610 36 1% 1/16W MF 402 — NEC_USB_DBP 25 37 39

VDD_PCI: H3 M4 C8
VDD: P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7
AVDD: N10 M12

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

39 37 24 18 12 9 PCI_AD<0>	M5	AD0	
39 37 24 18 12 9 PCI_AD<1>	P5	AD1	
39 37 24 18 12 9 PCI_AD<2>	N5	AD2	
39 37 24 18 12 9 PCI_AD<3>	P4	AD3	
39 37 24 18 12 9 PCI_AD<4>	N4	AD4	
39 37 24 18 12 9 PCI_AD<5>	M3	AD5	
39 37 24 18 12 9 PCI_AD<6>	N3	AD6	
39 37 24 18 12 9 PCI_AD<7>	M1	AD7	
39 37 24 18 12 9 PCI_AD<8>	L2	AD8	
39 37 24 18 12 9 PCI_AD<9>	L1	AD9	
39 37 24 18 12 9 PCI_AD<10>	K2	AD10	
39 37 24 18 12 9 PCI_AD<11>	L3	AD11	
39 37 24 18 12 9 PCI_AD<12>	K1	AD12	
39 37 24 18 12 9 PCI_AD<13>	K3	AD13	
39 37 24 18 12 9 PCI_AD<14>	J2	AD14	
39 37 24 18 12 9 PCI_AD<15>	J1	AD15	
39 37 24 18 12 9 PCI_AD<16>	F2	AD16	
39 37 24 18 12 9 PCI_AD<17>	E3	AD17	
39 37 24 18 12 9 PCI_AD<18>	E1	AD18	
39 37 24 18 12 9 PCI_AD<19>	D3	AD19	
39 37 24 18 12 9 PCI_AD<20>	D1	AD20	
39 37 24 18 12 PCI_AD<21>	D2	AD21	
39 37 24 18 12 PCI_AD<22>	C2	AD22	
39 37 24 18 12 PCI_AD<23>	C1	AD23	
39 37 24 18 12 9 PCI_AD<24>	B4	AD24	
39 37 24 18 12 9 PCI_AD<25>	A4	AD25	
39 37 24 18 12 9 PCI_AD<26>	B5	AD26	
39 37 24 18 12 9 PCI_AD<27>	C4	AD27	
39 37 24 18 12 9 PCI_AD<28>	A5	AD28	
39 37 24 18 12 9 PCI_AD<29>	C5	AD29	
39 37 24 18 12 9 PCI_AD<30>	B6	AD30	
39 37 24 18 12 9 PCI_AD<31>	A6	AD31	
37 24 18 12 PCI_CBE<0>	M2	CBE0	
37 24 18 12 PCI_CBE<1>	J3	CBE1	
37 24 18 12 PCI_CBE<2>	F1	CBE2	
37 24 18 12 PCI_CBE<3>	C3	CBE3	
39 37 24 18 12 PCI_PAR	J4	PAR	
39 37 24 18 12 PCI_FRAME_L	F3	FRAME	
39 37 24 18 12 PCI_IRDY_L	F4	IRDY	
39 37 24 18 12 PCI_TRDY_L	G1	TRDY	
39 37 24 18 12 PCI_STOP_L	G3	STOP	
NEC_IDSEL	B3	IDSEL	
39 37 24 18 12 PCI_DEVSEL_L	G2	DEVSEL	
12 NEC_PCI_REQ_L	C6	REQ	
12 NEC_PCI_GNT_L	D6	GNT	
18 PCI_PERR_L	H2	PERR	
18 PCI_SERR_L	H1	SERR	OD
NEC_PCI_INTA_L	C7	INTA	OD
NEC_PCI_INTB_L	B7	INTB	OD
NEC_PCI_INTC_L	A7	INTC	OD
35 12 CLK33M_NEC	A8	PCLK	
17 NEC_IO_RESET_L	B8	VBBRST	
NEC_CRUN_L	N6	CRUN	
17 NEC_PME_L	D9	PME	OD
17 NEC_MAIN_RESET_L	C9	VCCRST	
NEC_SMI_L_TP	L6	SMI	OD
17 NEC_LEGC	L7	LEGC	

R636 22 5% 1/16W MF 402
Series Rpaks required to facilitate NAND-tree testing
RP45 47 5% SM1 — 14 NEC_PCI_INT_L
R617 4.7K 5% 1/16W MF 402
RP44 47 5% SM1
29 26 23 IO_RESET_L — NEC_IO_RESET_L 17
39 29 24 14 PMU_PME_L — NEC_PME_L 17
39 29 24 19 18 14 MAIN_RESET_L — NEC_MAIN_RESET_L 17
17 NEC_LEGC

VSS: B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

XT1/SCLK	L9	NEC_XT1	
XT2	P8	NEC_XT2	
RSDM1	M14	NEC_USB_RSDM1	
DM1	M13	(NEC_USB_DAM)	
DP1	L14	(NEC_USB_DAP)	
RSDP1	K13	NEC_USB_RSDP1	
RSDM2	K14	NEC_USB_RSDM2	
DM2	K12	(NEC_USB_DBM)	
DP2	J14	(NEC_USB_DBP)	
RSDP2	J12	NEC_USB_RSDP2	
RSDM3	H11	NC	
DM3	G11		
DP3	G13		
RSDP3	G14	NC	
RSDM4	F12	NC	
DM4	F14		
DP4	E12		
RSDP4	E14	NC	
RSDM5	E13	NC	
DM5	D14		
DP5	C13		
RSDP5	C14	NC	
RREF	P11	NEC_RREF	
OCI1	B12	NEC_LUSB_OCI 17	
OCI2	B11	NEC_RUSB_OCI 17	
OCI3	B10	NEC_OCI<3>	
OCI4	A10	NEC_OCI<4>	
OCI5	B9	NEC_OCI<5>	
PPON1	C12 OUT	NEC_LUSB_PPON 25 39	
PPON2	A11 OUT	NEC_RUSB_PPON 25 39	
PPON3	C11 OUT	NEC_PPON3_TP	
PPON4	C10 OUT	NEC_PPON4_TP	
PPON5	A9 OUT	NEC_PPON5_TP	
NC1	P6	NEC_NC<1>	
NC2	M6	NEC_NC<2>	
NTEST1	M8 IPD	NC	
SMC	M7 IPD	NC	
TEB	N7 IPD	NC	
AMC	P7 IPD	NEC_AMC_TP	
TEST	L8 IPD	NC	
NANDTEST	M10	NEC_NANDTESTEN_TP	
SRCLK	M9	NC	
SRDTA	N9	NEC_NANDTESTOUT_TP	
SRMOD	P9 IPD	NC	
AVSS			
AVSS(R)	N11 P13 M12		

R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11
NEC_AVSS_F 17
R798 0 5% 1/10W MF 603

RP43 10K 5% 1/16W SM1 — +3V_NEC_VDD 17 38
RP43 10K 5% 1/16W SM1 — NEC_OCI<4>
R606 10K 5% 1/16W MF 402 — NEC_OCI<5>
R615 1K 5% 1/16W MF 402 — NEC_PPON3_TP
R632 1K 5% 1/16W MF 402 — NEC_PPON4_TP

NEC documentation indicates that NCs must be tied high.

+3V_MAIN
RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402 — 17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 25 39
R608 0 5% 1/16W MF 402 — 17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 25 39
NO STUFF C743 0.1UF 20% 10V CERM 402
NO STUFF C744 0.1UF 20% 10V CERM 402

USB 2.0

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PCI1510 PULL-UPS

+3V_SLEEP

R718 10K 5% 1/16W MF 402 — PCI_PERR_L (17 18)

R714 10K 5% 1/16W MF 402 — PCI_SERR_L (17 18)

R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU (18)

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805

C786 0.22uF 20% 6.3V CERM 402

C60 10uF 20% 6.3V CERM 805

C776 10uF 20% 6.3V CERM 805

C789 0.22uF 20% 6.3V CERM 402

C791 0.22uF 20% 6.3V CERM 402

C784 0.22uF 20% 6.3V CERM 402

C782 0.22uF 20% 6.3V CERM 402

C783 0.22uF 20% 6.3V CERM 402

C778 0.22uF 20% 6.3V CERM 402

C775 0.22uF 20% 6.3V CERM 402

R721 10K 5% 1/16W MF 402

A7 C13 D5 E1 M1 N7 N11 — VCC

+3V_MAIN

+5V_MAIN

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

U4 TPS2211 SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15		
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

+VPP_CBUS_SW (18 38)

+VCC_CBUS_SW (18 38)

C40 0.1uF 20% 10V CERM 402

C37 0.1uF 20% 10V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

(26 34 28 33 32) SLEEP_L_LS5

R726 0 5% 1/16W MF 402

TPS2211_SHTDWN_L

PCI1510_VR_EN_L

NC H10 CLK_48_RSVD/NC

DA VR_EN*

L8 VR_PORT

CRITICAL — CLAMP FOR PC-CARD — CLAMP FOR PCI

U8 PCI1510GGU BGA

VCCCB	B11		
VCCP	L3		
VCCD0*	N13	CBUS_VCCD0_L	
VCCD1*	L12	CBUS_VCCD1_L	
VPPD0	K9	CBUS_VPPD0	
VPPD1	M11	CBUS_VPPD1	
CD1*/CCD1*	L13	CBUS_DET_1_L	(18 39)
CD2*/CCD2*	B5	CBUS_DET_2_L	(18 39)
IORD*/CAD13	F12	CBUS_IORD_L	(18)
IOWR*/CAD15	C11	CBUS_IOWR_L	(18)
OE*/CAD11	G10	CBUS_OE_L	(18)
CE1*/CC/BE0*	H13	CBUS_CE1_L	(18)
VS1*/CVS1	B2	CBUS_VS1	(18)
VS2*/CVS2	A9	CBUS_VS2	(18)
WE*/CGNT*	D13	CBUS_WE_L	(18)
RDY/IREQ*/CINT*	A6	CBUS_READY	(18)
RESET/CRST*	D8	CBUS_RESET_L	(18)
REG*/CC/BE3*	A8	CBUS_REG_L	(18)
BVD1/CSTSCHG/STSCHG*/RI*	C6	CBUS_BVD1_L	(18)
BVD2/SPKR*/CAUDIO	D6	CBUS_BVD2_L	(18)
WP/IOIS16*/CCLKRUN*	A5	CBUS_WP_L	(18)
CE2/CAD10*	G13	CBUS_CE2_L	(18)
INPACK/CREQ*	B8	CBUS_INPACK_L	(18)
WAIT/CSERR*	B6	CBUS_WAIT_L	(18)
A0/CAD26	C7	CBUS_ADDR<0>	(18)
A1/CAD25	D7	CBUS_ADDR<1>	(18)
A2/CAD24	B7	CBUS_ADDR<2>	(18)
A3/CAD23	D10	CBUS_ADDR<3>	(18)
A4/CAD22	B12	CBUS_ADDR<4>	(18)
A5/CAD21	C8	CBUS_ADDR<5>	(18)
A6/CAD20	C9	CBUS_ADDR<6>	(18)
A7/CAD18	A12	CBUS_ADDR<7>	(18)
A8/CC/BE1*	E11	CBUS_ADDR<8>	(18)
A9/CAD14	F11	CBUS_ADDR<9>	(18)
A10/CAD9	G11	CBUS_ADDR<10>	(18)
A11/CAD12	G12	CBUS_ADDR<11>	(18)
A12/CC/BE2*	D9	CBUS_ADDR<12>	(18)
A13/CPAR	E12	CBUS_ADDR<13>	(18)
A14/CPERR*	D12	CBUS_ADDR<14>	(18)
A15/CIRDY*	C10	CBUS_ADDR<15>	(18)
A16/CCLK	B13	CBUS_ADDR_16_UF	
A17/CAD16	F10	CBUS_ADDR<17>	(18)
A18/RSVD	E13	CBUS_ADDR<18>	(18)
A19/CBLOCK*	A13	CBUS_ADDR<19>	(18)
A20/CSTOP*	E10	CBUS_ADDR<20>	(18)
A21/CDEVSEL*	D11	CBUS_ADDR<21>	(18)
A22/CTRDY*	C12	CBUS_ADDR<22>	(18)
A23/CFRAME*	A10	CBUS_ADDR<23>	(18)
A24/CAD17	B10	CBUS_ADDR<24>	(18)
A25/CAD19	B9	CBUS_ADDR<25>	(18)
D0/CAD27	A4	CBUS_DATA<0>	(18)
D1/CAD29	C4	CBUS_DATA<1>	(18)
D2/RSVD	A3	CBUS_DATA<2>	(18)
D3/CAD0	K11	CBUS_DATA<3>	(18)
D4/CAD1	K12	CBUS_DATA<4>	(18)
D5/CAD3	J13	CBUS_DATA<5>	(18)
D6/CAD5	J10	CBUS_DATA<6>	(18)
D7/CAD7	H12	CBUS_DATA<7>	(18)
D8/CAD28	C5	CBUS_DATA<8>	(18)
D9/CAD30	B4	CBUS_DATA<9>	(18)
D10/CAD31	B3	CBUS_DATA<10>	(18)
D11/CAD2	M12	CBUS_DATA<11>	(18)
D12/CAD4	J11	CBUS_DATA<12>	(18)
D13/CAD6	K13	CBUS_DATA<13>	(18)
D14/RSVD	J12	CBUS_DATA<14>	(18)
D15/CAD8	H11	CBUS_DATA<15>	(18)

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> (18)

R719 22 5% 1/16W MF 402

R723 47 5% 1/16W MF 402 — MAIN_RESET_L (29 24 19 17 14)

PCI_AD<19> (39 37 24 17 12 9) — (PCI_AD<19>)

PCI_AD<0>	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
(PCI_AD<19>)	H2	AD19
PCI_AD<20>	G2	AD20
PCI_AD<21>	G4	AD21
PCI_AD<22>	F1	AD22
PCI_AD<23>	C3	AD23
PCI_AD<24>	F3	AD24
PCI_AD<25>	E2	AD25
PCI_AD<26>	F4	AD26
PCI_AD<27>	B1	AD27
PCI_AD<28>	D2	AD28
PCI_AD<29>	E4	AD29
PCI_AD<30>	D3	AD30
PCI_AD<31>	E3	AD31
PCI_CBE<0>	K6	C/BE0*
PCI_CBE<1>	M3	C/BE1*
PCI_CBE<2>	J2	C/BE2*
PCI_CBE<3>	A1	C/BE3*
PCI_PAR	N1	PAR
PCI_IRDY_L	K1	IRDY
PCI_SERR_L (18 17)	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
PCI_PERR_L (18 17)	K3	PERR
PCI_FRAME_L	J1	FRAME
PCI_STOP_L	L1	STOP
PCI_TRDY_L	J3	TRDY
PCI_DEVSEL_L	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L (12)	C2	REQ
CBUS_PCI_GNT_L (12)	C1	GNT
CLK33M_CBUS (35 12)	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU (18)	N10	SUSPEND
CBUS_INT_L (14)	K7	MFUNC0
CBUS_MFUNC1_PD (18)	N9	MFUNC1
CBUS_MFUNC2_PD (18)	L9	MFUNC2
CBUS_MFUNC3_PD (18)	K10	MFUNC3
CBUS_MFUNC4_PD (18)	M10	MFUNC4
CBUS_MFUNC5_PD (18)	N12	MFUNC5
CBUS_MFUNC6_PD (18)	L10	MFUNC6
	L11	GRST

RP1 10K 5% 1/32W 25V (SM)

6	CBUS_MFUNC1_PD (18)
4	CBUS_MFUNC2_PD (18)
7	CBUS_MFUNC3_PD (18)
3	CBUS_MFUNC4_PD (18)
9	CBUS_MFUNC5_PD (18)
8	CBUS_MFUNC6_PD (18)
2	
1	

5 — 10

GND: A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL

J5 QT500806-L111 M-ST-SM

	2	1	CBUS_DATA<3> (18)
(39 18) CBUS_DET_1_L	4	3	CBUS_DATA<4> (18)
(18) CBUS_DATA<11>	6	5	CBUS_DATA<5> (18)
(18) CBUS_DATA<12>	8	7	CBUS_DATA<6> (18)
(18) CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> (18)
(18) CBUS_DATA<14>	14	13	CBUS_CE1_L (18)
(18) CBUS_DATA<15>	16	15	CBUS_ADDR<10> (18)
(18) CBUS_CE2_L	18	17	CBUS_OE_L (18)
(18) CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> (18)
(18) CBUS_IORD_L	24	23	CBUS_ADDR<9> (18)
(18) CBUS_IOWR_L	26	25	CBUS_ADDR<8> (18)
(18) CBUS_ADDR<17>	28	27	CBUS_ADDR<13> (18)
(18) CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> (18)
(18) CBUS_ADDR<19>	34	33	CBUS_WE_L (18)
(18) CBUS_ADDR<20>	36	35	CBUS_READY (18)
(18) CBUS_ADDR<21>	38	37	+VCC_CBUS_SW (18 38)
(38 18) +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW (18 38)
(38 18) +VPP_CBUS_SW	44	43	CBUS_ADDR<16> (18)
(18) CBUS_ADDR<22>	46	45	CBUS_ADDR<15> (18)
(18) CBUS_ADDR<23>	48	47	CBUS_ADDR<12> (18)
(18) CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> (18)
(18) CBUS_ADDR<25>	54	53	CBUS_ADDR<6> (18)
(18) CBUS_VS2	56	55	CBUS_ADDR<5> (18)
(18) CBUS_RESET_L	58	57	CBUS_ADDR<4> (18)
(18) CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> (18)
(18) CBUS_INPACK_L	64	63	CBUS_ADDR<2> (18)
(18) CBUS_REG_L	66	65	CBUS_ADDR<1> (18)
(18) CBUS_BVD2_L	68	67	CBUS_ADDR<0> (18)
(18) CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> (18)
(18) CBUS_DATA<8>	74	73	CBUS_DATA<1> (18)
(18) CBUS_DATA<9>	76	75	CBUS_DATA<2> (18)
(18) CBUS_DATA<10>	78	77	CBUS_WP_L (18)
(39 18) CBUS_DET_2_L	80	79	

84 81 — 83 82

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 20% 10V CERM 805

C800 2.2uF 20% 10V CERM 805

CARDBUS

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D	401243	0A
SCALE: NONE	SHT 18 OF 44	

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SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

L22 60-OHM-EMI (SM) — GPU_VCORE

C476 0.01uF 20% 16V CERM 402
C457 0.01uF 20% 16V CERM 402
C458 10uF 20% 6.3V CERM 805
C490 0.01uF 20% 16V CERM 402
C442 0.01uF 20% 16V CERM 402
C530 0.01uF 20% 16V CERM 402

GPU_VCORE_VDDCI

CRITICAL
U47 RAGE_MOBILITY M10-CSP64 64MB BGA (6 OF 6)
VSS, VDDCI

CRITICAL
U47 RAGE_MOBILITY M10-CSP64 64MB BGA (1 OF 6)

AGP_AD<31:0> AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

AGP_CBE<3:0> CBEB3 CBEB2 CBEB1 CBEB0

CLK66M_GPU_AGP PCICLK
AGP_FRAME_L FRAMEB
AGP_IRDY_L IRDYB
AGP_TRDY_L TRDYB
AGP_STOP_L STOPB
AGP_DEVSEL_L DEVSELB
AGP_PAR PAR
AGP_REQ_L REQB
AGP_GNT_L GNTB
AGP_ATI_INT_L INTAB
AGP_ATI_RESET_L RSTB
AGP_WBF_L WBF

AGP_ATI_VREFG VREFG
AGP_ATI_VREF VREF

AD_STB0 AGP_AD_STB<0>
AD_STB1 AGP_AD_STB<1>
AD_STBB0 AGP_AD_STB_L<0>
AD_STBB1 AGP_AD_STB_L<1>
AGP_BUSYB AGP_BUSY_L
AGPREF INT_AGP_VREF
AGPTEST GPU_AGP_TEST
AGP8X_DETB AGP8X_DET_PU

SUS_STAT AGP_SUS_STAT_L_PU

ST0 AGP_ST<0>
ST1 AGP_ST<1>
ST2 AGP_ST<2>

SBA7 AGP_SBA<7>
SBA6 AGP_SBA<6>
SBA5 AGP_SBA<5>
SBA4 AGP_SBA<4>
SBA3 AGP_SBA<3>
SBA2 AGP_SBA<2>
SBA1 AGP_SBA<1>
SBA0 AGP_SBA<0>
RBFB AGP_RBF_L

STP_AGPB AGP_STP_L
SB_STB AGP_SB_STB
SB_STBS AGP_SB_STB_L
RSTB_MSK ATI_RSTB_MSK

DBI_LO ATI_DBI_LO_PU
DBI_HI ATI_DBI_HI_PU

TEST_YCLK
TEST_MLCK
MEMTEST ATI_MEMTEST
PLLTEST NC

D+ GPU_THERM_DP
D- GPU_THERM_DM
GPU_MEM_IO

MEMVMODE0
MEMVMODE1

R323 10K 5% 1/16W MF 402 — +3V_GPU
R313 47 1% 1/16W MF 402 — +1_5V_AGP
R338 20K 5% 1/16W MF 402
C412 0.01uF 20% 16V CERM 402
C408 0.1uF 20% 10V CERM 402 (PLACE C408 CLOSE TO AGPREF PIN)
R335 20K 5% 1/16W MF 402 — +3V_GPU
R336 0 5% 1/16W MF 402
R325 47K 5% 1/16W MF 402 — +1_5V_AGP
R324 47K 5% 1/16W MF 402
R372 45.3 1% 1/16W MF 402

R337 10K 5% 1/16W MF 402 — +3V_GPU
MAIN_RESET_L IS TOGGLED FOR SLEEP
R309 47 5% 1/16W MF 402 — MAIN_RESET_L
R388 1K 1% 1/16W MF 402 — +3V_GPU
R397 1K 1% 1/16W MF 402 — GPU_MEM_IO
R373 1K 1% 1/16W MF 402
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
R365 1K 1% 1/16W MF 402
C516 0.1uF 20% 16V CERM 402
C508 10uF 20% 6.3V CERM 805

+1_8V_GPU
R370 4.7K 5% 1/16W MF 402
R371 4.7K 5% 1/16W MF 402
R375 4.7K 5% 1/16W MF 402
R376 4.7K 5% 1/16W MF 402

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

CRITICAL
U47 RAGE_MOBILITY M10-CSP64 64MB BGA (2 OF 6)
VSS

+3V_SLEEP
L78 400-OHM-EMI (SM-1)
L79 400-OHM-EMI (SM-1)
L80 400-OHM-EMI (SM-1)
C854 10uF 20% 6.3V CERM 805
C855 10uF 20% 6.3V CERM 805
C856 10uF 20% 6.3V CERM 805
C857 100pF 5% 50V CERM 402
C858 100pF 5% 50V CERM 402
C859 100pF 5% 50V CERM 402
C860 100pF 5% 50V CERM 402
C861 100pF 5% 50V CERM 402
C862 100pF 5% 50V CERM 402
C863 10uF 20% 6.3V CERM 805
+3V_SI_AVCC
+3V_SI_PLLVCC
+3V_SI_VCC
PLL NOISE SHOULD BE LESS THAN 100mV PEAK-TO-PEAK

MAIN_RESET_L
R835 10K 5% 1/16W MF 402
R832 47 5% 1/16W MF 402
R833 47 5% 1/16W MF 402 — NO STUFF
R818 10K 5% 1/16W MF 402 — NO STUFF
R823 10K 5% 1/16W MF 402
R825 10K 5% 1/16W MF 402

SI_I2C_CLK
SI_I2S_DATA
SI_I2S
SI_RST_L
SI_PD_L
SI_HPD

U58 SIL1162 TSSOP

SCL/DK1 SDA/DK0 CTL3/A2 ISEL/RST* PD* EDGE/HTPLG
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
DE HSYNC VSYNC IDCK+ IDCK-
PVCC1 PVCC2 AVCC AVCC AVCC VCC VCC
PGND PGND AGND AGND AGND GND GND GND THRML PAD

MSEN — SI_MSEN
R837 4.99K 1% 1/16W MF 402
R826 330 5% 1/16W MF 402

TXC+ TXC- TX0+ TX0- TX1+ TX1- TX2+ TX2-
SI_TMDS_CLKP SI_TMDS_CLKN SI_TMDS_DP<0> SI_TMDS_DN<0> SI_TMDS_DP<2> SI_TMDS_DP<1> SI_TMDS_DN<1> SI_TMDS_DP<2> SI_TMDS_DN<2>

EXT_SWING — SI_EXT_SWING_SET (SET TO HIGH SWING MODE)
VREF — SI_VREF_IDCK_N
+1_8V_GPU

R819 10K 5% 1/16W MF 402 — NO STUFF
R824 10K 5% 1/16W MF 402 — NO STUFF
R836 10K 5% 1/16W MF 402
RP49 0K EXT_TMDS
RP50 0K EXT_TMDS
RP51 0K EXT_TMDS
RP60 0K EXT_TMDS

ATI_DVOD<1:0> GPU_DVOD<1:0>
ATI_DVOD<3:2> GPU_DVOD<3:2>
ATI_DVOD<7:6> GPU_DVOD<7:6>
ATI_DVOD<5:4> GPU_DVOD<5:4>
ATI_DVOD<10:9> GPU_DVOD<10:9>
ATI_DVOD<11:8> GPU_DVOD<11:8>
ATI_DVO_HSYNC GPU_DVO_HSYNC
ATI_DVO_VSYNC GPU_DVO_VSYNC
ATI_DVOD_DE GPU_DVOD_DE
ATI_DVO_CLKP GPU_DVO_CLKP

Place C879 close to SI pin#2
C879 0.1uF 20% 16V CERM 402
R838 1K 1% 1/16W MF 402
R839 1K 1% 1/16W MF 402

R827 300 5% 1/16W MF 402 — NO STUFF — TMDS_CLKP / TMDS_CLKN
C875 470pF 10% 50V CERM 402 — NO STUFF
C877 470pF 10% 50V CERM 402 — NO STUFF
C865 0.1uF 20% 16V CERM 402 — SI_TMDS_CLK_STM
R828 300 5% 1/16W MF 402 — NO STUFF — TMDS_DP<0> / TMDS_DN<0>
C871 470pF 10% 50V CERM 402 — NO STUFF
C873 470pF 10% 50V CERM 402 — NO STUFF
C864 0.1uF 20% 16V CERM 402 — SI_TMDS_D0_STM
R829 300 5% 1/16W MF 402 — NO STUFF — TMDS_DP<1> / TMDS_DN<1>
C876 470pF 10% 50V CERM 402 — NO STUFF
C878 470pF 10% 50V CERM 402 — NO STUFF
C866 0.1uF 20% 16V CERM 402 — SI_TMDS_D1_STM
R830 300 5% 1/16W MF 402 — NO STUFF — TMDS_DP<2> / TMDS_DN<2>
C872 470pF 10% 50V CERM 402 — NO STUFF
C874 470pF 10% 50V CERM 402 — NO STUFF
C867 0.1uF 20% 16V CERM 402 — SI_TMDS_D2_STM

RP56 10 5% 1/16W SM1 — SI_TMDS_CLKP / SI_TMDS_CLKN → TMDS_CLKP / TMDS_CLKN
RP52 10 5% 1/16W SM1 — SI_TMDS_DP<0> / SI_TMDS_DN<0> → TMDS_DP<0> / TMDS_DN<0>
RP57 10 5% 1/16W SM1 — SI_TMDS_DP<1> / SI_TMDS_DN<1> → TMDS_DP<1> / TMDS_DN<1>
RP53 10 5% 1/16W SM1 — SI_TMDS_DP<2> / SI_TMDS_DN<2> → TMDS_DP<2> / TMDS_DN<2>
RP58 0 5% 1/16W SM1 — GPU_TMDS_CLKN / GPU_TMDS_CLKP → TMDS_CLKN / TMDS_CLKP
RP54 0 5% 1/16W SM1 — GPU_TMDS_DN<0> / GPU_TMDS_DP<0> → TMDS_DN<0> / TMDS_DP<0>
RP59 0 5% 1/16W SM1 — GPU_TMDS_DN<1> / GPU_TMDS_DP<1> → TMDS_DN<1> / TMDS_DP<1>
RP55 0 5% 1/16W SM1 — GPU_TMDS_DN<2> / GPU_TMDS_DP<2> → TMDS_DN<2> / TMDS_DP<2>

27M OSC
(PLACE THE OSCILLATOR AND R304 AND R305 CLOSE TO ATI PIN AJ29)
+3V_SLEEP
L16 FERR-EMI-100-OHM (SM)
R304 100K 5% 1/16W MF 402 — NO STUFF
C409 0.1uF 20% 16V CERM 402
C401 4.7uF 20% 6.3V CERM 805
CRITICAL VCC G1 27.0000M OSC SM-1 OE OUT GND
ATI_OSC_OE
+3V_ATI_OSC_SLEEP
ATI_CLK27M_OSC
ATI_CLK27M_OSC_SS
R305 0 5% 1/16W MF 402
R315 287 1% 1/16W MF 402 (PLACE R315 CLOSE TO OSC)
R320 162 1% 1/16W MF 402
ATI_CLK27M_IN

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD
+3V_SLEEP
L66 FERR-EMI-100-OHM (SM)
+3V_ATI_SS
C384 10uF 20% 6.3V CERM 805
C390 0.1uF 20% 16V CERM 402
R289 0 5% 1/16W MF 402 — NO STUFF
R297 0 5% 1/16W MF 402
R290 0 5% 1/16W MF 402 — NO STUFF
R298 0 5% 1/16W MF 402 — NO STUFF
CY25811_S1
CY25811_S0
U30 CY25811 SO1 VDD XIN/CLKIN XOUT SSCLK FRSEL S1 S0 VSS
ATI_SSCLK_UF
R285 33 5% 1/16W MF 402
ATI_SSCLK_IN

M10 AGP INTERFACE

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SCALE: NONE	SHT 19 OF 44	

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Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
R374 162 1% 1/16W MF 402 — GPU_TMDS_CLKP
R377 162 1% 1/16W MF 402 — GPU_TMDS_CLKN
C536 470pF 10% 50V CERM 402
C522 470pF 10% 50V CERM 402

GPU_TMDS_D0_CMF
R367 162 1% 1/16W MF 402 — GPU_TMDS_D0P
R369 162 1% 1/16W MF 402 — GPU_TMDS_D0N
C515 470pF 10% 50V CERM 402
C507 470pF 10% 50V CERM 402

GPU_TMDS_D1_CMF
R362 162 1% 1/16W MF 402 — GPU_TMDS_D1P
R355 162 1% 1/16W MF 402 — GPU_TMDS_D1N
C487 470pF 10% 50V CERM 402
C497 470pF 10% 50V CERM 402

GPU_TMDS_D2_CMF
R350 162 1% 1/16W MF 402 — GPU_TMDS_D2P
R340 162 1% 1/16W MF 402 — GPU_TMDS_D2N
C479 470pF 10% 50V CERM 402
C469 470pF 10% 50V CERM 402

R765 10 5% 1/16W MF 402 — GPU_TMDS_D0N
R760 10 5% 1/16W MF 402 — GPU_TMDS_D0P
R762 10 5% 1/16W MF 402 — GPU_TMDS_D1N
R764 10 5% 1/16W MF 402 — GPU_TMDS_D1P
R766 10 5% 1/16W MF 402 — GPU_TMDS_D2N
R761 10 5% 1/16W MF 402 — GPU_TMDS_D2P
R763 10 5% 1/16W MF 402 — GPU_TMDS_CLKP

Place all TMDS 10 ohms close to GPU

R389 10K 5% 1/16W MF 402 — +1_8V_GPU, +3V_GPU
R840 10K 5% 1/16W MF 402 — EXT_TMDS
ZV_LCDDATA20_PU

R378 1K 5% 1/16W MF 402

NO STUFF R380 10K 5% 1/16W MF 402 — +3V_GPU
HPD_PWR_SNS_EN
GPU_VCORE_CNTL_L

R351 1K 5% 1/16W MF 402 — ATI_TESTEN

U47 RAGE_MOBILITY M10-CSP64 64MB BGA (3 OF 6)

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_B	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	GPU_HPD
AUXWIN	AJ27	AUXWIN_PU
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_I2S_DATA
DDC3CLK	AH25	SI_I2C_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC
VSS	A20	
VSS	B21	

ZV_LCDDATA0	AJ5	ATI_DVOD<0>
ZV_LCDDATA1	AK5	ATI_DVOD<1>
ZV_LCDDATA2	AG6	ATI_DVOD<2>
ZV_LCDDATA3	AH6	ATI_DVOD<3>
ZV_LCDDATA4	AJ6	ATI_DVOD<4>
ZV_LCDDATA5	AK6	ATI_DVOD<5>
ZV_LCDDATA6	AG7	ATI_DVOD<6>
ZV_LCDDATA7	AH7	ATI_DVOD<7>
ZV_LCDDATA8	AJ7	ATI_DVOD<8>
ZV_LCDDATA9	AK7	ATI_DVOD<9>
ZV_LCDDATA10	AG8	ATI_DVOD<10>
ZV_LCDDATA11	AH8	ATI_DVOD<11>
ZV_LCDDATA12	AJ8	NC
ZV_LCDDATA13	AK8	NC
ZV_LCDDATA14	AG9	NC
ZV_LCDDATA15	AH9	NC
ZV_LCDDATA16	AJ9	NC
ZV_LCDDATA17	AK9	NC
ZV_LCDDATA18	AG10	NC
ZV_LCDDATA19	AH10	NC
ZV_LCDDATA20	AJ10	ZV_LCDDATA20_PU
ZV_LCDDATA21	AK10	NC
ZV_LCDDATA22	AG11	NC
ZV_LCDDATA23	AH11	NC
ZV_LCDCNTL0	AJ4	ATI_DVO_VSYNC
ZV_LCDCNTL1	AK4	ATI_DVO_HSYNC
ZV_LCDCNTL2	AH5	ATI_DVOD_DE
ZV_LCDCNTL3	AG5	ATI_DVO_CLKP
GPIO0	AJ2	ATI_AGP_FBSKEW<0>
GPIO1	AK2	ATI_AGP_FBSKEW<1>
GPIO2	AK1	ATI_X1CLK_SKEW<0>
GPIO3	AH3	ATI_X1CLK_SKEW<1>
GPIO4	AH2	ATI_BUS_CFG<0>
GPIO5	AJ1	ATI_BUS_CFG<1>
GPIO6	AF4	ATI_BUS_CFG<2>
GPIO7	AH1	ATI_GPIO7_SPN
GPIO8	AG3	ATI_GPIO8_PD
GPIO9	AF3	ATI_GPIO9_SPN
GPIO10	AG2	ATI_GPIO10_SPN
GPIO11	AF2	ATI_GPIO11_SPN
GPIO12	AG1	ATI_GPIO12_SPN
GPIO13	AF1	ATI_GPIO13_SPN
GPIO14	AE2	HPD_PWR_SNS_EN
GPIO15	AE1	GPU_VCORE_CNTL_L
GPIO16	M1	ATI_SSCLK_IN
TX0M	AJ13	ATI_TMDS_DN<0>
TX0P	AK13	ATI_TMDS_DP<0>
TX1M	AJ14	ATI_TMDS_DN<1>
TX1P	AK14	ATI_TMDS_DP<1>
TX2M	AJ15	ATI_TMDS_DN<2>
TX2P	AK15	ATI_TMDS_DP<2>
TXCM	AJ12	ATI_TMDS_CLKN
TXCP	AK12	ATI_TMDS_CLKP
XTALIN	AJ29	ATI_CLK27M_IN
XTALOUT	AJ30	NC
TESTEN	AH24	ATI_TESTEN
SSIN	AJ26	NC
VSS	B24	
VSS	B20	
VSS	A24	

Q23 SI3446DV TSOP

+1_5V_AGP → GPU_CORE_OK → +GPU_VDD15_UF

L17 FERR-220-OHM 0805 (500mA)

+1_5V_GPU_VDD15 → VDD15

C448 0.01uF, C443 0.01uF, C435 0.01uF, C482 0.01uF, C411 10uF 20% 16V CERM 805
C505 0.01uF, C532 0.01uF, C529 0.01uF, C526 0.01uF 20% 16V CERM 402
C407 1000pF 10% 25V X7R 402

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

GPU_VCORE

C484 10uF, C485 10uF 20% 6.3V CERM 805
C440 0.22uF, C441 0.22uF, C445 0.22uF, C446 0.22uF, C449 0.22uF, C434 0.22uF 20% 6.3V CERM 402
C452 0.22uF, C451 0.22uF, C494 0.22uF, C498 0.22uF, C509 0.22uF, C510 0.22uF, C512 0.22uF, C513 0.22uF 20% 6.3V CERM 402
C524 0.22uF, C525 0.22uF, C528 0.22uF, C531 0.22uF, C533 0.22uF, C477 0.22uF, C486 0.22uF, C495 0.22uF 20% 6.3V CERM 402

VDDC

R332 715 1% 1/16W MF 402
R333 499 1% 1/16W MF 402
R359 75 1% 1/16W MF 402
R356 75 1% 1/16W MF 402
R360 75 1% 1/16W MF 402

R779 10K 5% 1/16W MF 402 — +3V_GPU
R366 10K 5% 1/16W MF 402
R368 10K 5% 1/16W MF 402

M10 Power Shut down Sequencing

XW11 SM — DP5 BAS16TW SOT-363 — +1_8V_ATI_PVDD → +1_8V_PVDD_NECK
XW9 SM — +2_5V_SLEEP → +2_5V_SLEEP_NECK1
XW12 SM — DP5 BAS16TW SOT-363 — GPU_VCORE → GPU_VCORE_NECK
XW4 SM — +1_5V_AGP → +1_5V_AGP_NECK
XW5 SM — DP5 BAS16TW SOT-363 — +GPU_VDD15_UF → +GPU_VDD15_NECK

R384 10K, R387 10K, NO STUFF R386 10K, NO STUFF R382 10K, NO STUFF R383 10K, NO STUFF R385 10K, NO STUFF R381 10K 5% 1/16W MF 402 — +3V_GPU

(GPIO0)	ATI_AGP_FBSKEW<0>
(GPIO1)	ATI_AGP_FBSKEW<1>
(GPIO2)	ATI_X1CLK_SKEW<0>
(GPIO3)	ATI_X1CLK_SKEW<1>
(GPIO4)	ATI_BUS_CFG<0>
(GPIO5)	ATI_BUS_CFG<1>
(GPIO6)	ATI_BUS_CFG<2>

NO STUFF R393 10K, NO STUFF R396 10K, NO STUFF R395 10K, NO STUFF R391 10K, NO STUFF R392 10K, NO STUFF R394 10K, NO STUFF R390 10K 5% 1/16W MF 402

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

+PBUS

C706 4.7uF, C708 4.7uF 20% 25V CERM 1206

CRITICAL Q48 SI7860DP SO-8-PWRPK

CRITICAL L64 2.2uH-11A SM

D12 1N914 SOT23

D29 SM MBRS130LT3

CRITICAL Q49 IRF7832 SO-8

OMIT XW19 JUMPER OPEN — GPU_VCORE → GPU_VCORE_SW → GPU_VCORE_SW_F

CRITICAL C704 22uF 20% 10V CERM 1210
CRITICAL C707 330uF 20% 6.3V TANT CASE-D4
CRITICAL C705 330uF 20% 6.3V TANT CASE-D4
CRITICAL C711 330uF 20% 6.3V TANT CASE-D4

R329 4.99K 1% 1/16W MF 402
R328 18.2K 1% 1/16W MF 402 — GPU_PWRMSR
R330 20K 1% 1/16W MF 402
R361 1.82K 1% 1/16W MF 402 — GPU_PWRMSR

R786 100K 5% 1/16W MF 402 — +5V_MAIN, HIGH_VCORE_DIV
C846 0.1uF 20% 10V CERM 402 — GPU_PWRMSR
HIGH_VCORE
GPU_VCORE_CNTL_RC
GPU_VCORE_CNTL

Q25 2N7002DW SOT-363

R549 10K 5% 1/16W MF 402 — GPU_PWRMSR — GPU_VCORE_CNTL_L
C712 0.1uF 20% 10V CERM 402 — NO STUFF

R343 0 5% 1/16W MF 402
NO STUFF R352 63.4K 1% 1/16W MF 402
C466 4.7uF 20% 10V CERM 1206 — 1778_GND
R357 100K 5% 1/16W MF 402
R358 2.2 5% 1/16W MF 603 — 1778_BST_RC
C431 0.1uF 20% 25V CERM 603
C481 0.1uF 20% 25V CERM 603

EXT INI VIN
U32 LTC1778 SSOP
RUN/SS, ITH, VRNG, FCB, PGOOD, SGND, PGND, VCC, VCC, SW, TG, BOOST, BG, VFB, ION

R339 20K 1% 1/16W MF 402 — 1778_ITH_RC
C455 470pF 10% 50V CERM 402
C465 220pF 5% 25V CERM 402
NO STUFF R344 0 5% 1/16W MF 402
R353 0 5% 1/16W MF 402
C480 0.1uF 20% 10V CERM 402
NO STUFF C838 0.001uF 20% 50V CERM 402

OMIT XW6 SM

R327 1M 5% 1/16W MF 402
R331 1 5% 1/16W MF 603
R326 576K 1% 1/16W MF 402

R558 10K 5% 1/16W MF 402 — GPU_VCORE_SEQ_L
R555 33K 5% 1/16W MF 402
Q51 2N3904 SM — GPU_VCORE_SEQ
Q52 2N3904 SM — GPU_VCORE_SEQ
R559 100K 5% 1/16W MF 402 — GPU_VCORE_PWR_SEQ
R556 100K 5% 1/16W MF 402 — +1_5V_AGP
DP7 BAS16TW SOT-363 — SLEEP_L_LS5
DP7 BAS16TW SOT-363 — DCDC_EN

M10 CORE PWR/LVDS/TMDS

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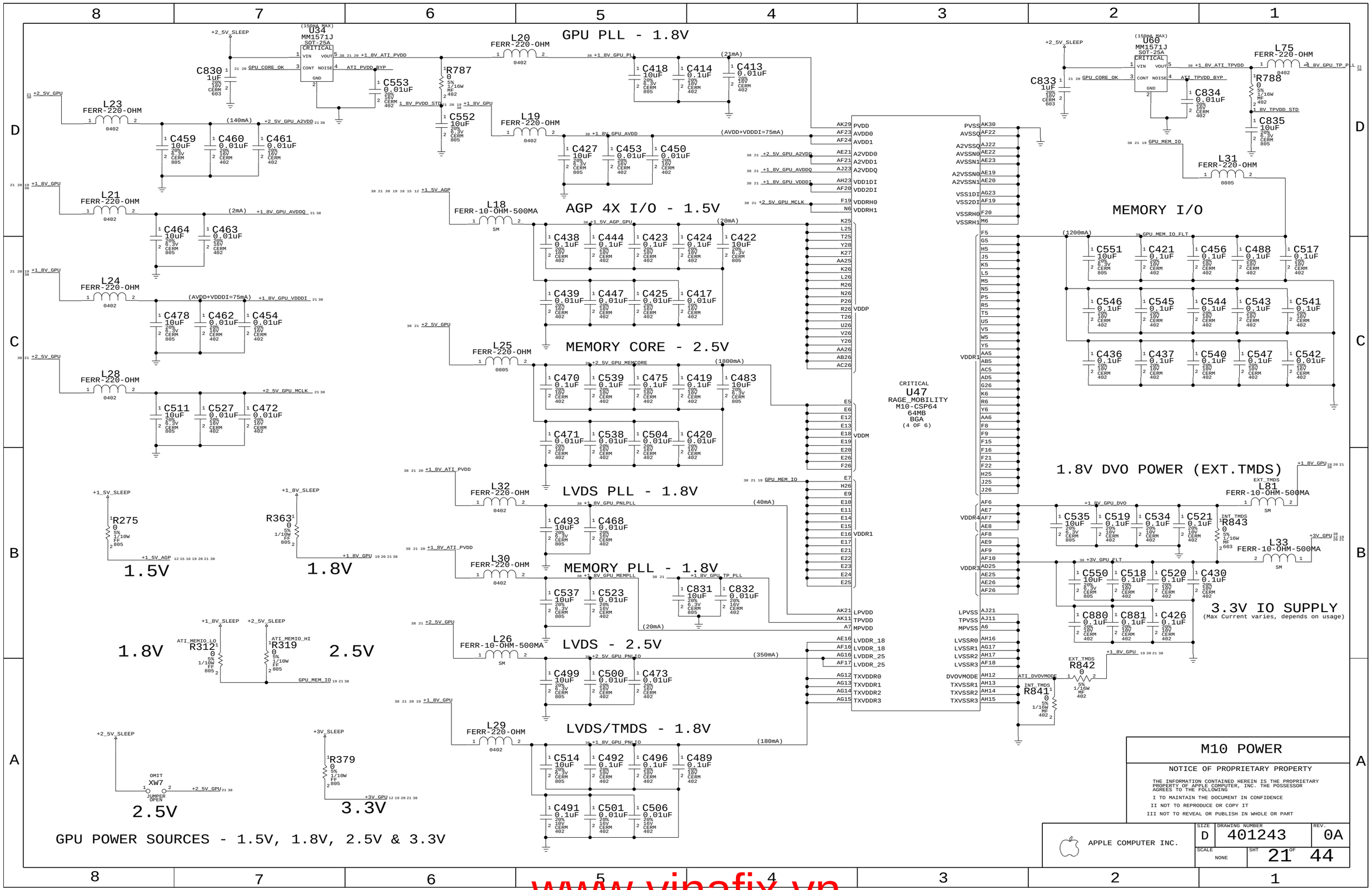
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SCALE: NONE	SHT 20 OF 44	

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EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN
74AHC1G32
U40
OMIT
L38 FERR-60-OHM-0.1A 0402
20 ATI_VSYNC
ATI_VSYNC_BUF
VGA_VSYNC 22 39

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

+3V_MAIN
74AHC1G32
U39
OMIT
L36 FERR-60-OHM-0.1A 0402
20 ATI_HSYNC
ATI_HSYNC_BUF
VGA_HSYNC 22 39

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 90-OHM-200MA SM CRITICAL
L46 90-OHM-200MA SM_VER-1 CRITICAL
L47 90-OHM-200MA SM_VER-1 CRITICAL

39 37 19 TMDS_DN<0> 2
39 37 19 TMDS_DP<0> 1
TMDS_CONN_DN<0>
TMDS_CONN_DP<0>
TMDS_DN<2> 39 37 19
TMDS_DP<2> 39 37 19
TMDS_DN<1> 39 37 19
TMDS_DP<1> 39 37 19

J22 QH1112 F-RT-TH CRITICAL
CHGND1

(TMDS_DN<5>)
(TMDS_DP<5>)
(TMDS_DN<4>)
(TMDS_DP<4>)
(TMDS_DN<3>)
(TMDS_DP<3>)

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L37 370-OHM SM_VER-1
37 19 TMDS_CLKP
37 19 TMDS_CLKN
TMDS_CONN_CLKP 22 36 39
TMDS_CONN_CLKN 22 36 39

39 36 22 TMDS_CONN_CLKP
39 36 22 TMDS_CONN_CLKN

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP
F2 0.5AMP-13.2V CRITICAL SM
38 +5V_DDC_SLEEP_UF
L42 400-OHM-EMI SM-1
+5V_DDC_SLEEP 22 38 39

Isolation required for DVI power switch

D19 MBR0530 SM
DDC_CLK_ISO
R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402
R477 100 5% 1/16W MF 402
R469 100 5% 1/16W MF 402
C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C667 0.01uF 20% 50V CERM 603
C653 100pF 5% 25V CERM 201
PLACE NEAR C5A & C5B
R464 0 5% 1/16W MF 402
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19
CHGND1
CHGND2

3V LEVEL SHIFTERS

+3V_SLEEP
Q39 2N7002DW SOT-363
Q40 2N7002DW SOT-363
R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402
DVI_DDC_CLK
DVI_DDC_DATA
DVI_HPD
GPU_DVI_DDC_CLK
GPU_DVI_DDC_DATA
GPU_HPD
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. since host rails will be low, TPS610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TPS610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q38 TP0610 SM
39 22 DVI_DDC_CLK_UF
39 38 22 +5V_DDC_SLEEP
DVI_TURN_ON
R473 680 5% 1/16W MF 402
DVI_TURN_ON_ILIM
R459 330 5% 1/16W MF 402
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
DVI_TURN_ON_BASE
R460 10K 5% 1/16W MF 402
Q35 MMDT3904 SOT-363
SOFT_PWR_ON_L 23 29 33 39

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R485 68.1K 1/16W MF 402
C668 0.1uF 20% 10V CERM 402
HPD_4V_REF
U42 LMC7211 SM
HPD_PWR_SW_BASE
R475 10K 5% 1/16W MF 402
Q35 MMDT3904 SOT-363
39 22 DVI_HPD_UF
R472 10K 1% 1/16W MF 402
DVI_HPD_DIV
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
HPD_PWR_SW
R470 330 5% 1/16W MF 402
HPD_REF_EN_L
Q40 2N7002DW SOT-363
20 HPD_PWR_SNS_EN
R483 470K 5% 1/16W MF 402

LCD INTERFACE
LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN
R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402
LCD_PWREN_L
+3V_LCD_SW 38
L27 FERR-250-OHM SM
+3V_LCD (LVDS DDC POWER)
C503 0.001uF 20% 50V CERM 402
TSOP SI3443DV Q29
LCD_DIGON_L
Q28 2N7002 SM
22 20 FP_PWR_EN
+3V_SLEEP
R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402
LVDS_DDC_CLK 20 22 39
LVDS_DDC_DATA 20 22 39

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

NO STUFF
C702 0.001uF 20% 50V CERM 402

C548 0.001uF 20% 50V CERM 402
CHGND4
J14 G-501973 F-RT-SM CRITICAL

LVDS_DDC_CLK
LVDS_DDC_DATA
LVDS_L0N
LVDS_L0P
LVDS_L1N
LVDS_L1P
LVDS_L2N
LVDS_L2P
CLKLVDS_LN
CLKLVDS_LP
LVDS_U0N
LVDS_U0P
LVDS_U1N
LVDS_U1P
LVDS_U2N
LVDS_U2P
CLKLVDS_UN
CLKLVDS_UP

C549 0.001uF 20% 50V CERM 402

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM
+14V_INV
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW 38
L74 400-OHM-EMI SM-1
R750 100K 5% 1/16W MF 402
FP_PWR_EN_L
C812 0.001uF 20% 50V CERM 402
C813 10uF 20% 6.3V CERM 805
J4 SM-2MT CRITICAL
+5V_INV_SW
Q76 FDG6324L SC70-6
22 20 FP_PWR_EN
L72 400-OHM-EMI SM-1
BRIGHT_PWM
C815 0.001uF 20% 50V CERM 402
+3V_MAIN
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
INV_GND
L1 FERR-250-OHM SM
C22 0.1uF 20% 16V CERM 402
20 INV_ON_PWM
NC7S32 SC70
U2
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 50V CERM 603
CHGND3

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM
GPU_TV_GND1 38
L54 FERR-10-OHM-500MA SM
TV_GND1 38 39
C657 0.01uF 20% 50V CERM 603
L53 3.3uH 0603
20 GPU_Y
C663 560pF 10% 50V CERM 402
C656 560pF 10% 50V CERM 402
TV_C 39
L57 3.3uH 0603
20 GPU_C
C661 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
TV_Y 39
L55 3.3uH 0603
20 GPU_COMP
C664 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
TV_COMP 39
CRITICAL
J21 MINIDIN RT-TH MH11773-WMR8A
CHGND1
XW14 SM
GPU_TV_GND2 38
L56 FERR-10-OHM-500MA SM
TV_GND2 38 39
C659 0.01uF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

VIDEO CONNECTORS

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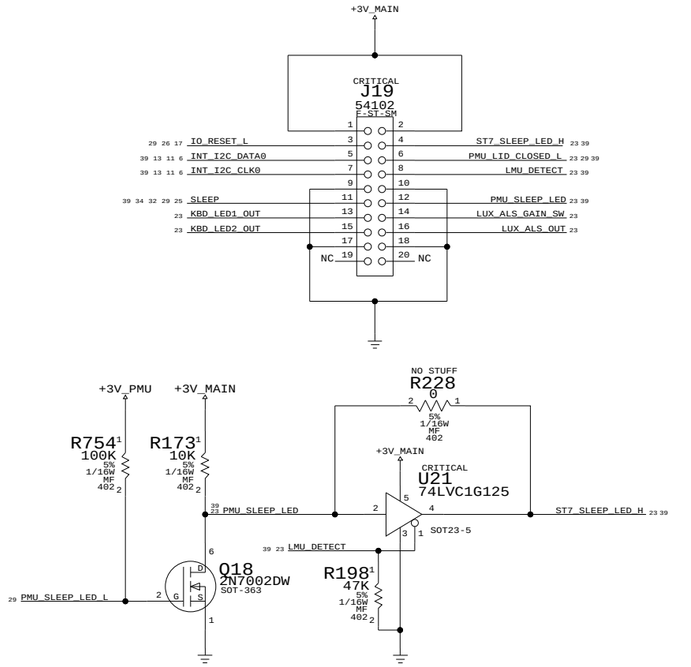
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

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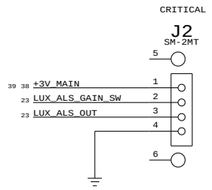
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D	401243	0A
SCALE: NONE	SHT 22 OF 44	

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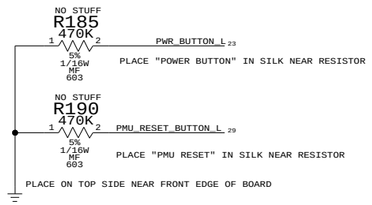
LMU/RIGHT SENSOR CONNECTOR



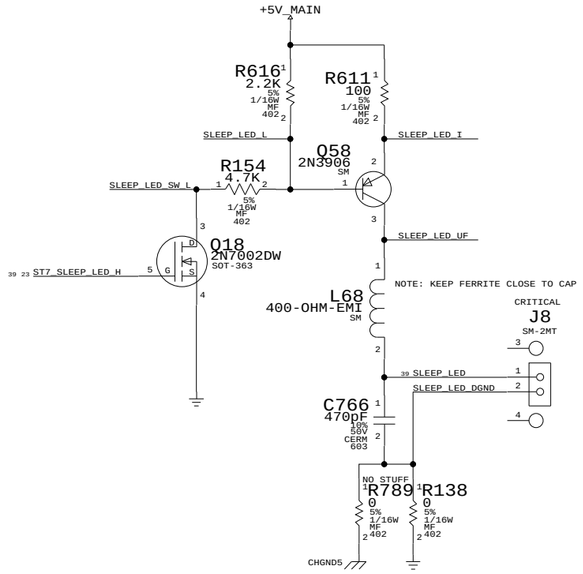
LEFT LIGHT SENSOR CONNECTOR



DEBUG HELPERS

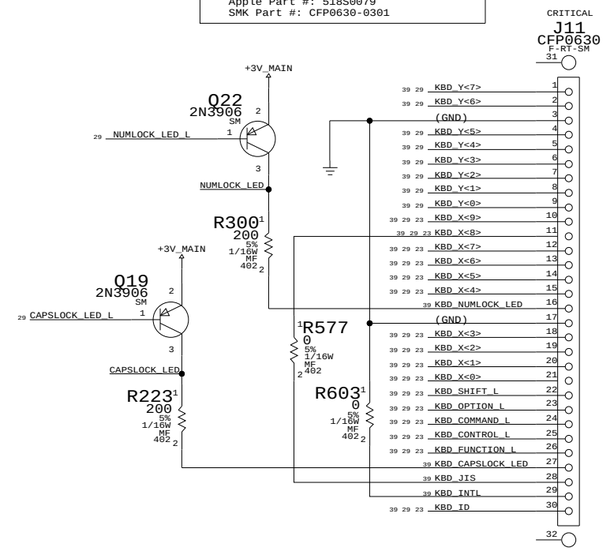


SLEEP LED

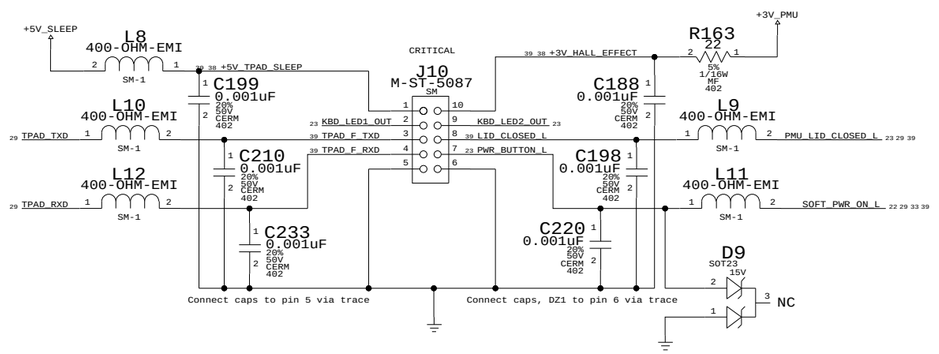


TOP CONTACT ZIF KEYBOARD CONN

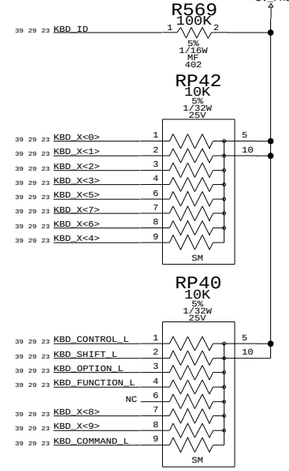
CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301



TRACKPAD/PWR BTN CONN



KEYBOARD PULLUPS



KEYBOARD/TPAD/SLEEP LED

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SCALE	SHT	OF
NONE	23	44

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EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

RP26 33 5% 1/16W SM1
EIDE_DATA<8> → EIDE_OPTICAL_DATA<8>
RP27 33 5% 1/16W SM1
EIDE_DATA<10> → EIDE_OPTICAL_DATA<10>
RP26 33 5% 1/16W SM1
EIDE_DATA<9> → EIDE_OPTICAL_DATA<9>
RP30 33 5% 1/16W SM1
EIDE_DATA<11> → EIDE_OPTICAL_DATA<11>
RP24 33 5% 1/16W SM1
EIDE_DATA<12> → EIDE_OPTICAL_DATA<12>
RP30 33 5% 1/16W SM1
EIDE_DATA<14> → EIDE_OPTICAL_DATA<14>
RP27 33 5% 1/16W SM1
EIDE_DATA<13> → EIDE_OPTICAL_DATA<13>
RP30 33 5% 1/16W SM1
EIDE_DATA<15> → EIDE_OPTICAL_DATA<15>
RP26 33 5% 1/16W SM1
EIDE_DATA<2> → EIDE_OPTICAL_DATA<2>
RP24 33 5% 1/16W SM1
EIDE_DATA<1> → EIDE_OPTICAL_DATA<1>
RP24 33 5% 1/16W SM1
EIDE_DATA<0> → EIDE_OPTICAL_DATA<0>
RP27 33 5% 1/16W SM1
EIDE_DATA<3> → EIDE_OPTICAL_DATA<3>
RP24 33 5% 1/16W SM1
EIDE_DATA<6> → EIDE_OPTICAL_DATA<6>
RP27 33 5% 1/16W SM1
EIDE_DATA<7> → EIDE_OPTICAL_DATA<7>
RP26 33 5% 1/16W SM1
EIDE_DATA<4> → EIDE_OPTICAL_DATA<4>
RP30 33 5% 1/16W SM1
EIDE_DATA<5> → EIDE_OPTICAL_DATA<5>
RP28 33 5% 1/16W SM1
EIDE_CS0_L → EIDE_OPTICAL_CS0_L
RP28 33 5% 1/16W SM1
EIDE_ADDR<1> → EIDE_OPTICAL_ADDR<1>
RP28 33 5% 1/16W SM1
EIDE_ADDR<2> → EIDE_OPTICAL_ADDR<2>
RP28 33 5% 1/16W SM1
EIDE_ADDR<0> → EIDE_OPTICAL_ADDR<0>
R234 10K 5% 1/16W MF 402

R266 33 5% 1/16W MF 402
EIDE_CS1_L → EIDE_OPTICAL_CS1_L
R237 82 5% 1/16W MF 402
EIDE_DMARQ → EIDE_OPTICAL_DMA_RQ
R238 22 5% 1/16W MF 402
EIDE_DMACK_L → EIDE_OPTICAL_DMACK_L
R262 22 5% 1/16W MF 402
EIDE_RD_L → EIDE_OPTICAL_READ_L
R268 22 5% 1/16W MF 402
EIDE_WR_L → EIDE_OPTICAL_WR_L
R251 82 5% 1/16W MF 402
EIDE_IOCHRDY → EIDE_OPTICAL_IOCHRDY
R217 82 5% 1/16W MF 402
EIDE_INT → EIDE_OPTICAL_INT
R242 33 5% 1/16W MF 402
EIDE_RST_L → EIDE_OPTICAL_RST_L

WIRELESS INTERFACE

+3V_SLEEP
NO STUFF R739 10K 5% 1/16W MF 402
CRITICAL J6 QT510806-L111 F-ST-SM
NO STUFF C808 100pF 5% 50V CERM 402
NO STUFF C805 100pF 5% 50V CERM 402

MAIN_RESET_L
RF_DISABLE_L
AIRPORT_PCI_REQ_L
PCI_AD<31>
PCI_AD<29>
PCI_AD<27>
PCI_AD<25>
PCI_CBE<3>
PCI_AD<23>
PCI_AD<21>
PCI_AD<19>
PCI_AD<17>
PCI_CBE<2>
PCI_IRDY_L
AIRPORT_CLKRUN_L
PCI_CBE<1>
PCI_AD<14>
PCI_AD<12>
PCI_AD<10>
ROM_RW_L
PCI_AD<8>
PCI_AD<7>
PCI_AD<5>
ROM_ONBOARD_CS_L
PCI_AD<3>
ROM_CS_L

CLK33M_AIRPORT
AIRPORT_PCI_GNT_L
PMU_PME_L
AIRPORT_PCI_INT_L
PCI_AD<30>
PCI_AD<28>
PCI_AD<26>
PCI_AD<24>
AIRPORT_IDSEL
PCI_AD<22>
PCI_AD<20>
PCI_PAR
PCI_AD<18>
PCI_AD<16>
PCI_FRAME_L
PCI_TRDY_L
PCI_STOP_L
PCI_DEVSEL_L
PCI_AD<15>
PCI_AD<13>
PCI_AD<11>
PCI_AD<9>
PCI_CBE<0>
ROM_OE_L
PCI_AD<6>
PCI_AD<4>
PCI_AD<2>
PCI_AD<0>

PCI_AD<18> → R737 22 5% 1/16W MF 402 → +3V_SLEEP

OPTICAL DRIVE INTERFACE (EIDE)

+5V_SLEEP
NO STUFF R541 100K 5% 1/16W MF 402
R540 10K 5% 1/16W MF 402
NO STUFF R546 10K 5% 1/16W MF 402
CRITICAL J13 SM-M

NC
EIDE_OPTICAL_RST_L
EIDE_OPTICAL_DATA<8>
EIDE_OPTICAL_DATA<9>
EIDE_OPTICAL_DATA<10>
EIDE_OPTICAL_DATA<11>
EIDE_OPTICAL_DATA<12>
EIDE_OPTICAL_DATA<13>
EIDE_OPTICAL_DATA<14>
EIDE_OPTICAL_DATA<15>
EIDE_OPTICAL_DMA_RQ
EIDE_OPTICAL_READ_L
EIDE_OPTICAL_DMAACK_L
EIDE_OPTICAL_ADDR<2>
EIDE_OPTICAL_CS1_L
NC
EIDE_OPTICAL_DATA<7>
EIDE_OPTICAL_DATA<6>
EIDE_OPTICAL_DATA<5>
EIDE_OPTICAL_DATA<4>
EIDE_OPTICAL_DATA<3>
EIDE_OPTICAL_DATA<2>
EIDE_OPTICAL_DATA<1>
EIDE_OPTICAL_DATA<0>
EIDE_OPTICAL_WR_L
EIDE_OPTICAL_IOCHRDY
EIDE_OPTICAL_INT
EIDE_OPTICAL_ADDR<1>
EIDE_OPTICAL_ADDR<0>
EIDE_OPTICAL_CS0_L
NC

R545 20K 5% 1/16W MF 402
R542 10K 5% 1/16W MF 402

PLACE SERIES R CLOSE TO INTERPID

UIDE_DATA<11> → RP19 33 5% 1/16W SM1 → HD_DATA<11>
UIDE_DATA<3> → RP18 33 5% 1/16W SM1 → HD_DATA<3>
UIDE_DATA<1> → RP18 33 5% 1/16W SM1 → HD_DATA<1>
UIDE_DATA<2> → RP18 33 5% 1/16W SM1 → HD_DATA<2>
UIDE_DATA<0> → RP18 33 5% 1/16W SM1 → HD_DATA<0>
UIDE_DATA<7> → RP19 33 5% 1/16W SM1 → HD_DATA<7>
UIDE_DATA<5> → RP19 33 5% 1/16W SM1 → HD_DATA<5>
UIDE_DATA<4> → RP19 33 5% 1/16W SM1 → HD_DATA<4>
UIDE_DATA<6> → RP21 33 5% 1/16W SM1 → HD_DATA<6>
UIDE_DATA<8> → RP21 33 5% 1/16W SM1 → HD_DATA<8>
UIDE_DATA<9> → RP23 33 5% 1/16W SM1 → HD_DATA<9>
UIDE_DATA<10> → RP21 33 5% 1/16W SM1 → HD_DATA<10>
UIDE_DATA<14> → RP23 33 5% 1/16W SM1 → HD_DATA<14>
UIDE_ADDR<0> → RP25 33 5% 1/16W SM1 → HD_ADDR<0>
UIDE_CS0_L → RP25 33 5% 1/16W SM1 → HD_CS0_L
UIDE_ADDR<1> → RP25 33 5% 1/16W SM1 → HD_ADDR<1>
UIDE_DATA<15> → RP23 33 5% 1/16W SM1 → HD_DATA<15>
UIDE_DATA<13> → RP21 33 5% 1/16W SM1 → HD_DATA<13>
UIDE_DATA<12> → RP25 33 5% 1/16W SM1 → HD_DATA<12>
UIDE_ADDR<2> → RP23 33 5% 1/16W SM1 → HD_ADDR<2>
UIDE_CS1_L → R214 33 5% 1/16W MF 402 → HD_CS1_L

R196 10K 5% 1/16W MF 402

PLACE PULLUP RESISTORS CLOSE TO INTREPID

+3V_SLEEP
R203 10K 5% 1/16W MF 402
R213 10K 5% 1/16W MF 402
R204 10K 5% 1/16W MF 402

UIDE_RST_L → R199 33 5% 1/16W MF 402 → HD_RESET_L
UIDE_DMACK_L → R229 22 5% 1/16W MF 402 → HD_DMACK_L
UIDE_DIOR_L → R200 22 5% 1/16W MF 402 → HD_DIOR_L
UIDE_DIOW_L → R215 22 5% 1/16W MF 402 → HD_DIOW_L
UIDE_IOCHRDY → R216 82 5% 1/16W MF 402 → HD_IOCHRDY

C284 10pF 5% 50V CERM 402

IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

HARD DRIVE INTERFACE (UATA100)

+3V_SLEEP
3V_HD_LOGIC R573 0 5% 1/16W MF 402
5V_HD_LOGIC R570 0 5% 1/16W MF 402
+5V_HD_SLEEP
CRITICAL J12 SM-M

HD_RESET_L
HD_DATA<7>
HD_DATA<6>
HD_DATA<5>
HD_DATA<4>
HD_DATA<3>
HD_DATA<2>
HD_DATA<1>
HD_DATA<0>
HD_DMARQ
HD_DIOR_L
HD_DMACK_L
HD_ADDR<1>
HD_ADDR<0>
HD_CS0_L
+HD_LOGIC_SLEEP

HD_DATA<8>
HD_DATA<9>
HD_DATA<10>
HD_DATA<11>
HD_DATA<12>
HD_DATA<13>
HD_DATA<14>
HD_DATA<15>
HD_DIOW_L
HD_INTRQ
HD_ADDR<2>
HD_CS1_L
HD_IOCHRDY

R579 20K 5% 1/16W MF 402
R578 10K 5% 1/16W MF 402

ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

INTERNAL I/O CONNECTORS

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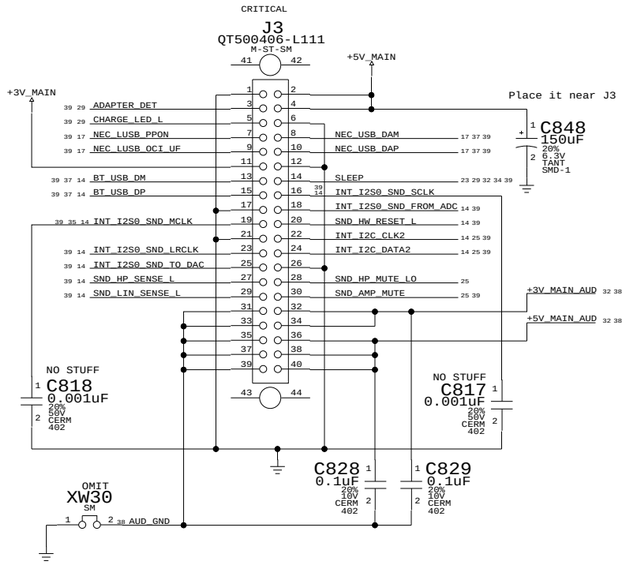
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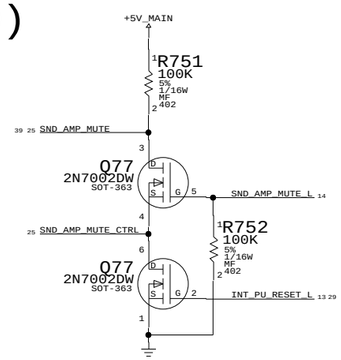
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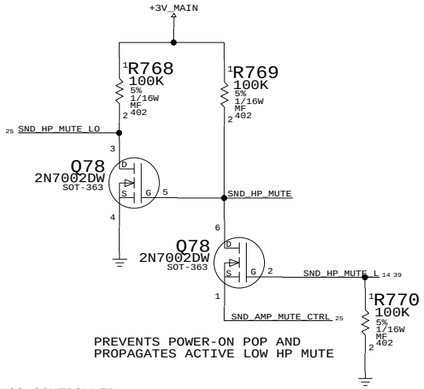
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LEFT I/O & AUDIO BOARD (LIO)



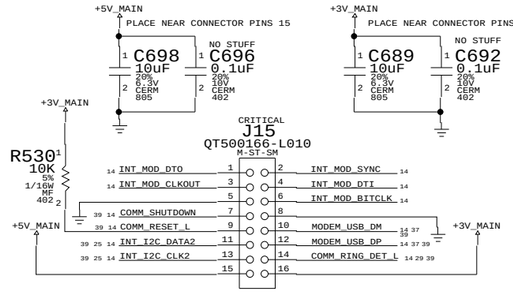


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



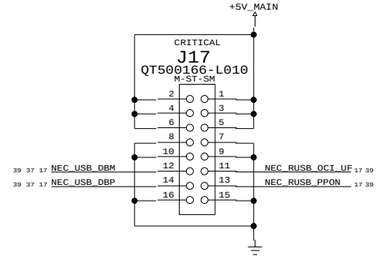
PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

USB MODEM/SOFT MODEM

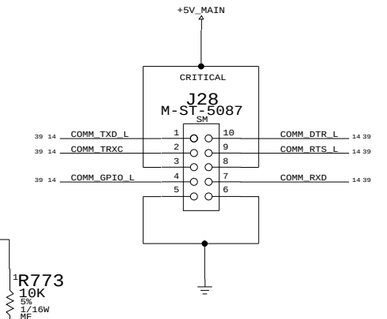


MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

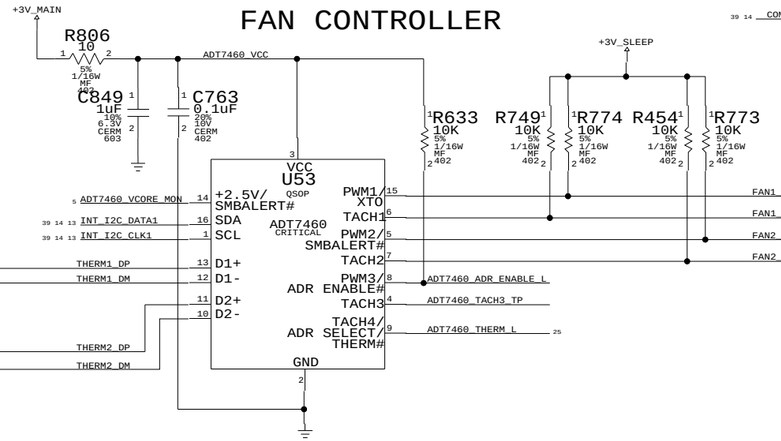


SERIAL DEBUG INTERFACE

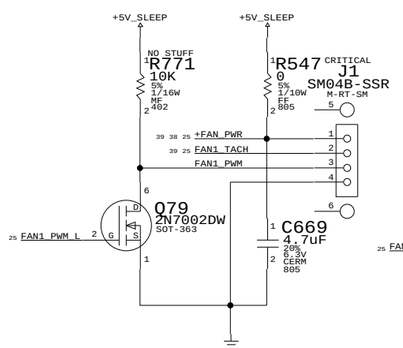


FAN INTERFACE

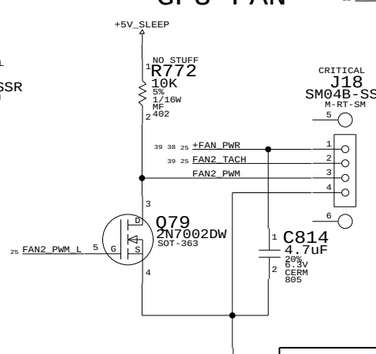
FAN CONTROLLER

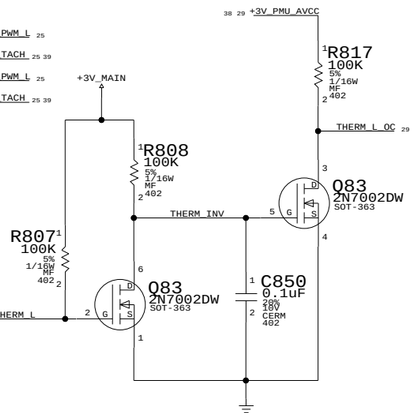


CPU FAN

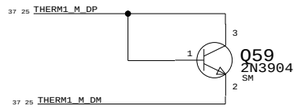


GPU FAN

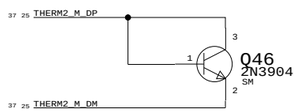




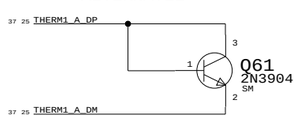
PLACE CLOSE TO CPU
MAIN1



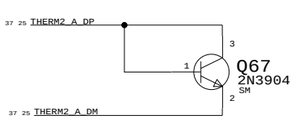
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



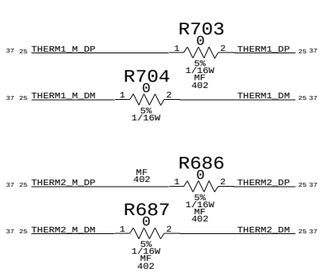
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



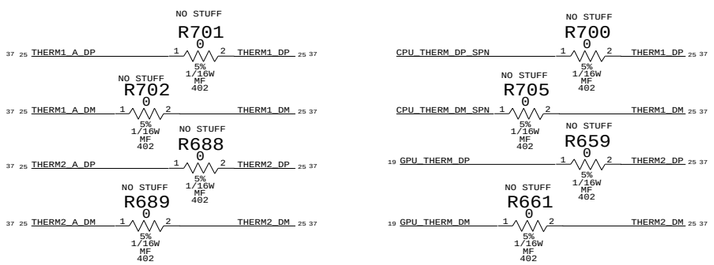
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



FAN/MODEM/SOUND/BACKUP BATT.

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Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/16W MF 402

3405_MODE

U45 LTC3405 SOT23-6 CRITICAL

VIN RUN MODE GND SW VFB

LTC3405_SW

CRITICAL L60 3.3uH SM1

R507 0 5% 1/16W MF 402

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

C674 10uF 20% 6.3V CERM 805

3405_VFB

+1_0V_MARVELL

R503 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402

R421 0 5% 1/16W MF 402

R445 0 5% 1/16W MF 402

CLKENET_LINK_TX

CLKENET_LINK_RX

CLKENET_LINK_GBE_REF

CLKENET_PHY_TX

CLKENET_PHY_RX

CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402

C852 10pF 5% 50V CERM 402

Keep C851 & C852 Stubs short

CRITICAL U43 88E1111 BCC

TX_CLK RX_CLK 125CLK

TXD0 TXD1 TXD2 TXD3 TXD4 TXD5 TXD6 TXD7

TX_EN TX_ER GTX_CLK

RXD0 RXD1 RXD2 RXD3 RXD4 RXD5 RXD6 RXD7

RX_DV RX_ER CRS COL MDC MDIO INT-/INT+ RESET COMA

S_IN+ S_IN- S_OUT+ S_OUT- S_CLK+ S_CLK- HSDAC+ HSDAC-

XTAL1 XTAL2 VSSC

CTRL10 NC

DVDD VDDO VDDOH VDDOX AVDD GND

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-

LED_LINK10 LED_LINK100 LED_LINK1000 LED_DUPLEX LED_RX LED_TX

CONFIG0 CONFIG1 CONFIG2 CONFIG3 CONFIG4 CONFIG5 CONFIG6

TDI TDO TCK TMS TRST

RSET

SEL_OSC SEL_2.5V

C611 2.2uF 20% 10V CERM 805

C594 0.1uF 20% 10V CERM 402

C601 0.01uF 20% 10V CERM 402

C608 0.1uF 20% 10V CERM 402

C619 0.01uF 20% 10V CERM 402

C603 0.1uF 20% 10V CERM 402

C599 0.01uF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

+2_5V_MARVELL

C597 0.1uF 20% 10V CERM 402

C612 0.01uF 20% 10V CERM 402

C623 0.1uF 20% 10V CERM 402

C600 0.01uF 20% 10V CERM 402

C598 0.1uF 20% 10V CERM 402

C595 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

L35 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

C614 0.1uF 20% 10V CERM 402

C616 0.01uF 20% 10V CERM 402

C618 0.1uF 20% 10V CERM 402

C602 0.01uF 20% 10V CERM 402

C592 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MAIN

R442 0 5% 1/16W MF 603

C646 0.1uF 20% 10V CERM 402

C648 0.1uF 20% 10V CERM 402

C645 0.1uF 20% 10V CERM 402

C647 0.1uF 20% 10V CERM 402

PLACE CAPS AT CONNECTOR PINS 5 & 6

CRITICAL J23 MJ-R0016 F-RT-TH

PRIMARY

ENET_CTAP ENET_CTAP MDI_0+ MDI_0- MDI_1+ MDI_1- MDI_2+ MDI_2- MDI_3+ MDI_3-

1CT:1CT 75 OHM

SECONDARY J1 J2 J3 J4 J5 J6 J7 J8

RJ45 CABLE SIDE

RJ45 CHIP SIDE

CHGND1

SHIELD 1000PF, 2000V

R433 49.9 1% 1/16W MF 402

R435 49.9 1% 1/16W MF 402

R437 49.9 1% 1/16W MF 402

R439 49.9 1% 1/16W MF 402

R434 49.9 1% 1/16W MF 402

R436 49.9 1% 1/16W MF 402

R438 49.9 1% 1/16W MF 402

R440 49.9 1% 1/16W MF 402

MDI0_PD MDI1_PD MDI2_PD MDI3_PD

C622 0.01uF 20% 10V CERM 402

C613 0.01uF 20% 10V CERM 402

C615 0.01uF 20% 10V CERM 402

C617 0.01uF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO PHY

SEE CONFIG TABLES (BELOW)

D15 1N914 SOT23

Q32 2N7002DW SOT-363

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

AC_IN

SLEEP_L LS5

IO_RESET_L

INT_ENET_RST_L

ENET_RST_L

ENET_COMA

ENET_ENERGY_DET

ENET_HSDACP

ENET_HSDACM

ENET_VSSC

ENET_RSET

JTAG_ENET_TDI

JTAG_ASIC_TDO_TP

JTAG_ASIC_TCK

JTAG_ASIC_TMS

JTAG_ASIC_TRST_L

R431 10K 5% 1/16W MF 402

R430 10K 5% 1/16W MF 402

R432 1.5K 5% 1/16W MF 402

R422 1K 5% 1/16W MF 402

NO STUFF R425 20K 5% 1/16W MF 402

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M

C604 27pF 5% 50V CERM 402

C624 27pF 5% 50V CERM 402

CLK25M_XTAL_IN

CLK25M_ENET_XIN

CLK25M_ENET_XOUT

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402

NO STUFF R429 49.9 1% 1/16W MF 402

R428 10K 5% 1/16W MF 402

R427 4.99K 1% 1/16W MF 402

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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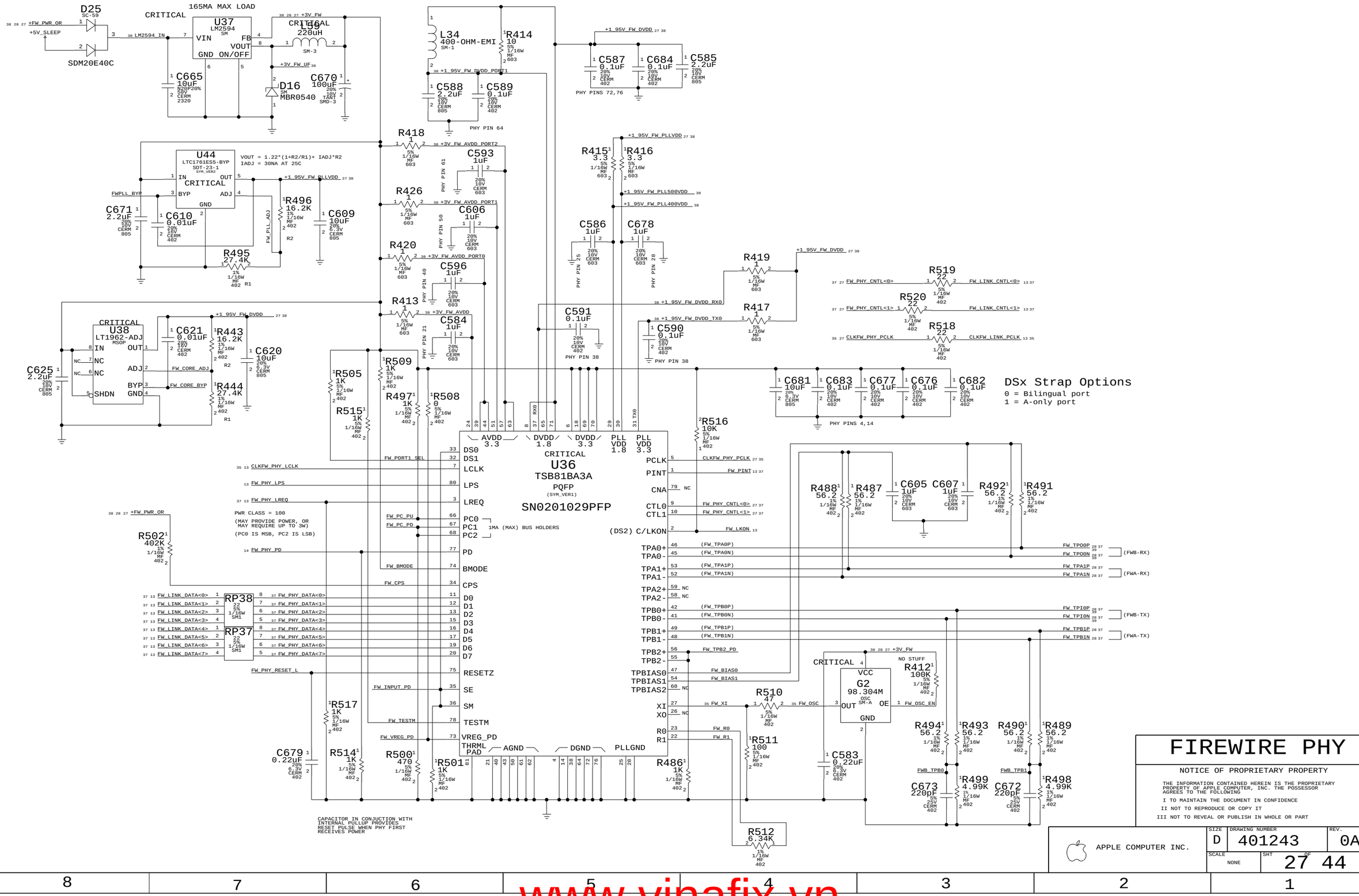
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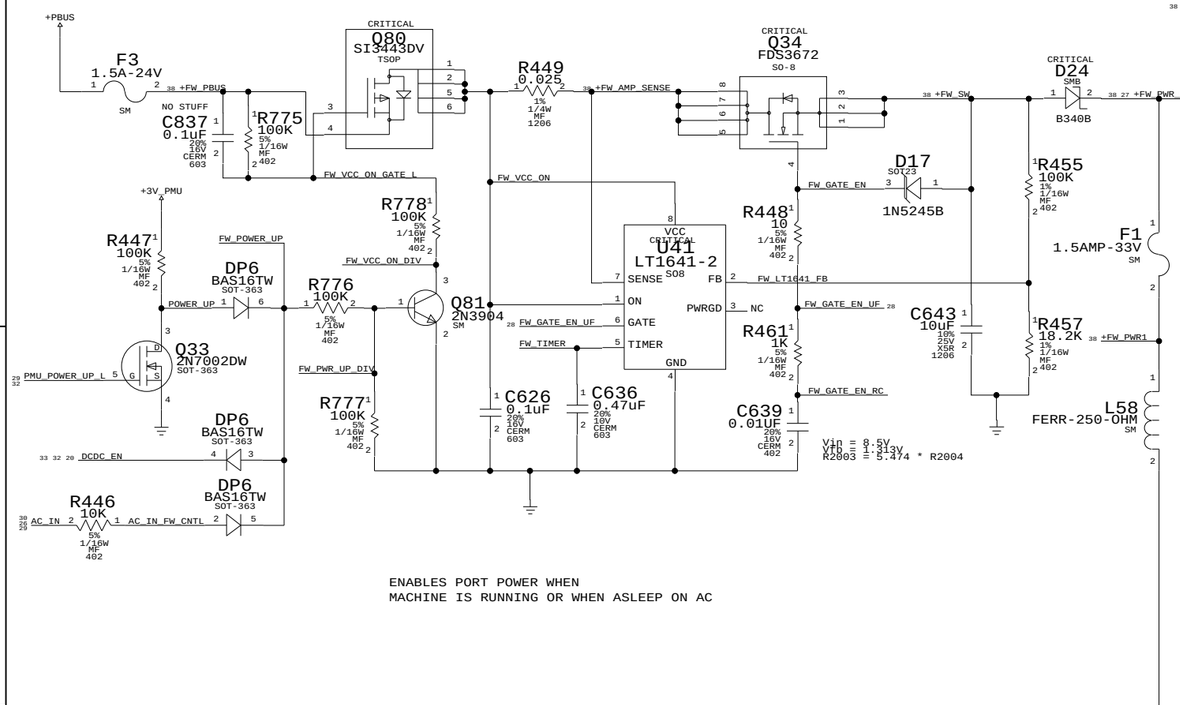
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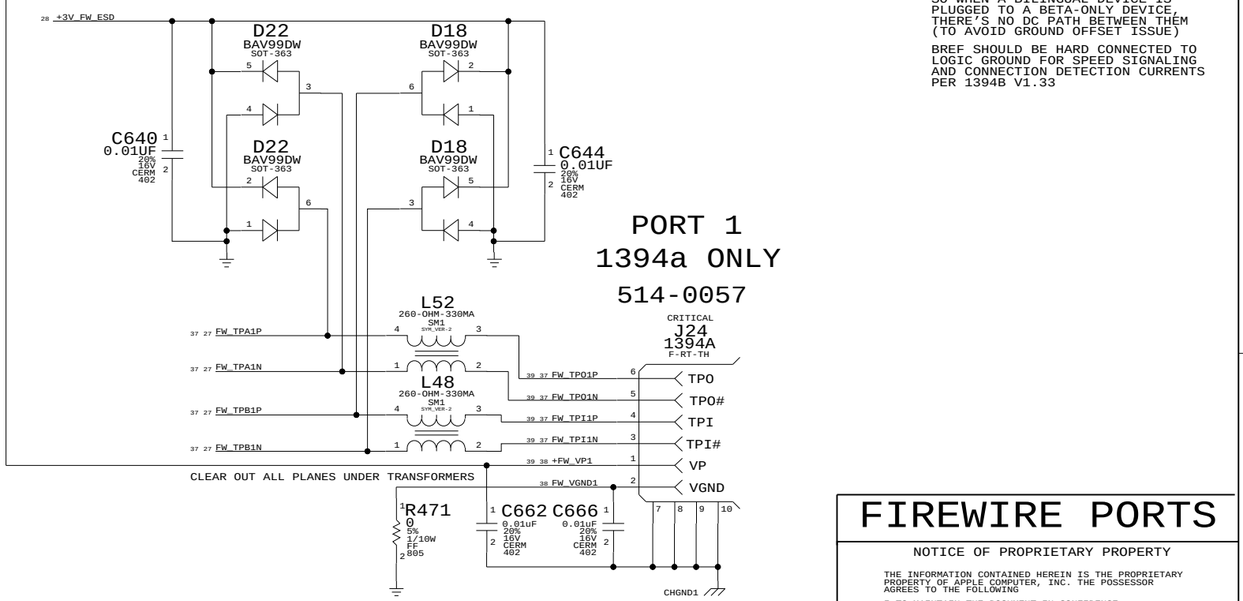
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PORT POWER SWITCH





FIREWIRE PORTS

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+3V_PMU
R595 470K 1 2 CHARGE_LED_L 25 29 39
R583 10K 1 2 PMU_POWER_UP_L 28 29 32
R582 10K 1 2 SOFT_PWR_ON_L 22 23 29 33 39
R560 100K 1 2 MAIN_RESET_L 14 17 18 19 24 29 39
RP39 100K 4 5 IO_RESET_L 17 23 26 29
RP39 100K 3 6 SLEEP 23 25 29 32 34 39
RP39 100K 1 8 INT_RESET_L 9 13 29
RP39 100K 2 7 INT_SUSPEND_REQ_L 8 29
R587 1K 2 1 PMU_BYTE 29
R586 10K 2 1 PMU_CNVSS 29
All 5% 1/16W MF 402 unless noted; RP39 SM1

+3V_PMU
C255 10uF 20% 6.3V CERM 805
C729 0.1uF 20% 10V CERM 402
C724 0.1uF 20% 10V CERM 402
R602 4.7 5% 1/16W MF 402
+3V_PMU_AVCC 25 29 38
C731 0.1uF 20% 10V CERM 402
VCC 14 60
AVCC 97

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U29	

CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. HLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

U29 M16C62 FLAS (OMIT)

KBD_Y<0> 39 23	86	P00_D0	P50_WRL_WR (PMU_AP)
KBD_Y<1> 39 23	85	P01_D1	P51_WRH_BHE
KBD_Y<2> 39 23	84	P02_D2	P52_RD
KBD_Y<3> 39 23	83	P03_D3	P53_BCLK
KBD_Y<4> 39 23	82	P04_D4	P54_HLDA
KBD_Y<5> 39 23	81	P05_D5	P55_HOLD
KBD_Y<6> 39 23	80	P06_D6	P56_ALE
KBD_Y<7> 39 23	79	P07_D7	P57_RDY_CLKOUT
PMU_NUMLOCK_LED_L	78	P10_D8	P60_CTS0_RTS0
PMU_CAPSLOCK_LED_L	77	P11_D9	P61_CLK0
CHARGE_LED_L 29 25 39	76	P12_D10	P62_RXD0
PMU_POWER_UP_L 29 28 39	75	P13_D11	P63_TXD0
NC	74	P14_D12	P64_CTS1_RTS1_CTS0_CLKS1
SOFT_PWR_ON_L 39 33 29 23 22	73	P15_D13_INT3	P65_CLK1
COMM_RING_DET_L 39 25 14	72	P16_D14_INT4	P66_RXD1
INT_WATCHDOG_L 14	71	P17_D15_INT5	P67_TXD1
KBD_X<0> 39 23	70	P20_A0_D0	P70_TXD2_SDA_TA0OUT
KBD_X<1> 39 23	69	P21_A1_D1_D0	P71_RXD2_SCL_TA0IN_TB5IN
KBD_X<2> 39 23	68	P22_A2_D2_D1	P72_CLK2_TA1OUT_V
KBD_X<3> 39 23	67	P23_A3_D3_D2	P73_CTS2_RTS2_TA1IN_V
KBD_X<4> 39 23	66	P24_A4_D4_D3	P74_TA2OUT_W
KBD_X<5> 39 23	65	P25_A5_D5_D4	P75_TA2IN_W
KBD_X<6> 39 23	64	P26_A6_D6_D5	P76_TA3OUT
KBD_X<7> 39 23	63	P27_A7_D7_D6	P77_TA3IN
KBD_X<8> 39 23	61	P30_A8_D7	P80_TA4OUT_U
KBD_X<9> 39 23	59	P31_A9	P81_TA4IN_U
IO_RESET_L 29 26 23 17	58	P32_A10	P82_INT0
KBD_COMMAND_L 39 23	57	P33_A11	P83_INT1
KBD_CONTROL_L 39 29 23	56	P34_A12	P84_INT2
KBD_SHIFT_L 39 29 23	55	P35_A13	P85_NMI
KBD_OPTION_L 39 29 23	54	P36_A14	P86_XCOUT
KBD_FUNCTION_L 39 23	53	P37_A15	P87_XCIN
PMU_INT_L 14	52	P40_A16	P90_TB0IN_CLK3
KBD_ID 39 23	51	P41_A17	P91_TB1IN_SIN3
CPU_PLL_STOP_OC 7	50	P42_A18	P92_TB2IN_SOUT3
NC	49	P43_A19	P93_DA0_TB3IN
SLEEP 39 34 32 29 25 23	48	P44_CS0	P94_DA1_TB4IN
	47	P45_CS1	P95_ANEX0_CLK4
INT_SUSPEND_ACK_L 8	46	P46_CS2	P96_ANEX1_SOUT4
INT_SUSPEND_REQ_L 29 8	45	P47_CS3	P97_ADTRG_SIN4
PMU_BYTE 29	6	BYTE	P100_AN0
CLK10M_PMU_XOUT	11	XOUT	P101_AN1
CLK10M_PMU_XIN	13	XIN	P102_AN2
PMU_RESET_L	10	RESET	P103_AN3
+3V_PMU_AVCC 38 29 25	96	VREF	P104_AN4_KI0
PMU_CNVSS 29	7	CNVSS	P105_AN5_KI1
		VSS 12 62	P106_AN6_KI2
			P107_AN7_KI3
			AVSS 94

CPU_VCORE_HI_OC	7 33	44	
INT_RESET_L	9 13 29	43	
MAIN_RESET_L	14 17 18 19 24 29 39	42	
NC		41	
PMU_INT_NMI	14	40	
PMU_EPM	29	39	
INT_PU_RESET_L	13 25 29	38	
PMU_CPU_HRESET_L	6 39	37	
PMU_ACK_L	14	36	
PMU_CLK	14	35	
PMU_FROM_INT	14	34	
PMU_TO_INT	14	33	
PMU_REQ_L	14	32	
PMU_LID_CLOSED_L	23 29 39	31	
PMU_RESET_BUTTON_L	23 29	30	
PMU_NMI_BUTTON_L	29	29	
TPAD_RXD	23 29	28	
TPAD_TXD	23 29	27	
SYSTEM_CLK_EN	14	26	
CPU_CLK_EN	8	25	
PMU_CHARGE_V	30	24	
PMU_CHRG_BATT_0	30	23	
NC (CHARGE_I)		22	
NC		21	
PMU_SLEEP_LED_L	23	20	
CPU_SMI_L	5	19	
POWER_VALID	29	18	
PMU_PME_L	14 17 24 29 39	17	
INT_PEND_PROC_INT	14	16	
PMU_NMI_L	29	15	
CLK32K_PMU_XOUT		9	
CLK32K_PMU_XIN		8	
PMU_BATT0_DET_L		5	
PMU_BATT1_DET_L_PU	29	4	
NC		3	
NC		2	
INT_PROC_SLEEP_REQ_L	14	1	
PMU_POWERUP_OK	29	100	
NC		99	
PMU_OOPS	29	98	
THERM_L_OC	25	95	
PMU_AC_IN	29	93	
PMU_AC_DET	29	92	
NC		91	
PMU_I2C_CLK	29	90	
PMU_I2C_DATA	29	89	
PMU_SMB_CLK	29 30	88	
PMU_SMB_DATA	29 30	87	

R597 2.2K 23 NUMLOCK_LED_L 1 2 PMU_NUMLOCK_LED_L
R596 2.2K 23 CAPSLOCK_LED_L 1 2 PMU_CAPSLOCK_LED_L
All 5% 1/16W MF 402

UNDERVOLTAGE RESET CIRCUIT

+3V_PMU
R267 1K 5% 1/16W MF 402 — 33 +3V_PMU_RESET
C370 0.1uF 20% 10V CERM 402
U26 MAX6804 SOT143: VCC 4, MR* 3 (39 29 PMU_KB_RESET_L), RSET* 2, GND 1
CLK10M_PMU_XOUT
CLK10M_PMU_XIN
NO STUFF R580 10M 5% 1/16W MF 402
R581 0 5% 1/16W MF 402
CRITICAL Y4 10.00M SM
CLK10M_PMU_XOUT_UF
C406 12pF 5% 50V CERM 402
C728 12pF 5% 50V CERM 402

Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0604		Y4	Alt crystal size

PMU KEYBOARD RESET CIRCUIT

+3V_PMU
U20 NC7S32 SC70: A 39 33 29 23 22 SOFT_PWR_ON_L, B 39 29 23 KBD_CONTROL_L, Y PMU_KB_RESET_IN1
U24 NC7S32 SC70: A 39 29 23 KBD_SHIFT_L, B 39 29 23 KBD_OPTION_L, Y PMU_KB_RESET_IN2
C277 0.1uF 20% 10V CERM 402
U25 NC7S32 SC70: A, B PMU_KB_RESET_IN1/IN2, Y PMU_KB_RESET_L 29 39

KEEP CAP CLOSE TO ALL 3 OR GATES

ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

Keep crystal subcircuit close to PMU.
CLK32K_PMU_XOUT
CLK32K_PMU_XIN
R588 1K 1 2 PMU_BATT_DET_L 29 30 39
R600 1K 1 2 AC_IN 26 28 30
NO STUFF R248 10M 1 2
R249 0 1 2
CRITICAL Y3 SM-2 32.768K 1 3 (2 4)
CLK32K_PMU_XOUT_UF
C339 12pF 5% 50V CERM 402
C340 12pF 5% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 12.5PF

+3V_PMU
38 31 +4.85V_RAW
R592 100K 1% 1/16W MF 402
R593 100K 1% 1/16W MF 402 — ADAPTER_DET 25 39
R590 402K 1% 1/16W MF 402 — PMU_AC_DET 29

A29 ADAPTER DETECTION

R348 5.23K 1% 1/16W MF 402
C467 0.1uF 20% 10V CERM 402
R364 10K 5% 1/16W MF 402 — A29_DETECT 30
U33 LMC7211 SM: A29_DET_REF, PMU_AC_DET, A29_DET_L 1
R345 499K 1% 1/16W MF 402
R349 12.7K 1% 1/16W MF 402
Q30 2N7002 SM: G, D, S

RP41 10K 29 PMU_EPM 4 5 — SM1
RP41 10K 29 23 PMU_RESET_BUTTON_L 3 6
R261 100K 29 PMU_POWERUP_OK 2 1
R591 470K 29 PMU_BATT1_DET_L_PU 2 1
R589 470K 39 30 29 PMU_BATT_DET_L 2 1
RP41 10K 29 PMU_NMI_BUTTON_L 2 7
RP41 10K 29 PMU_NMI_L 1 8
R584 7.15K 30 29 PMU_SMB_DATA 2 1 (1%)
R585 7.15K 30 29 PMU_SMB_CLK 2 1 (1%)
R599 10K 29 PMU_I2C_CLK 2 1 — +3V_SLEEP
R598 10K 29 PMU_I2C_DATA 2 1
R563 10K 29 23 IPAD_RXD 2 1 — +5V_SLEEP
R564 10K 29 23 IPAD_TXD 2 1
R576 100K 29 POWER_VALID 2 1 — +3V_MAIN
R575 10K 39 29 24 17 14 PMU_PME_L 2 1
R562 100K 39 29 23 PMU_LID_CLOSED_L 2 1
R594 10K 29 PMU_OOPS 1 2
R561 100K 29 25 13 INT_PU_RESET_L 1 2
All 5% 1/16W MF 402 unless noted

PMU

NOTICE OF PROPRIETARY PROPERTY

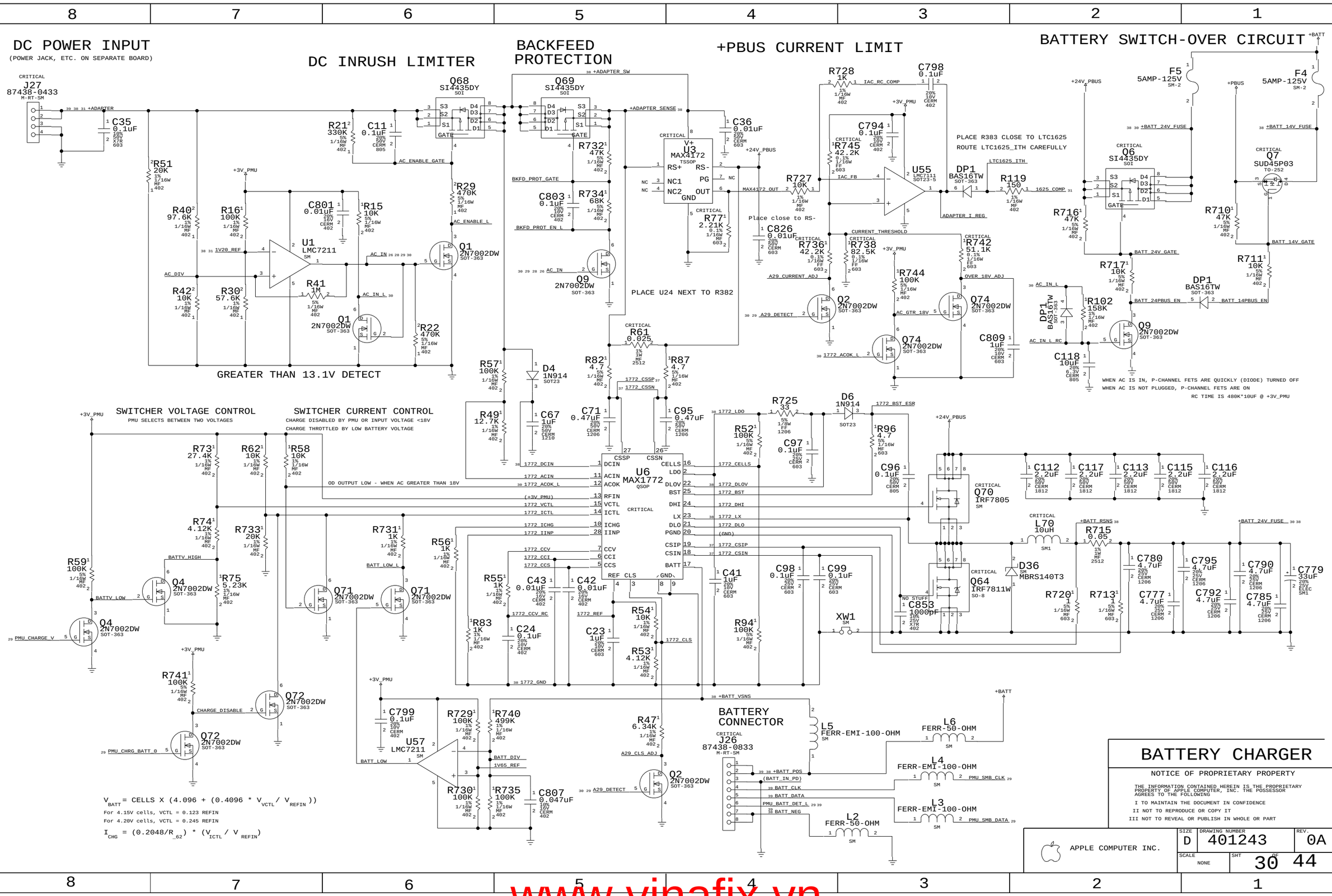
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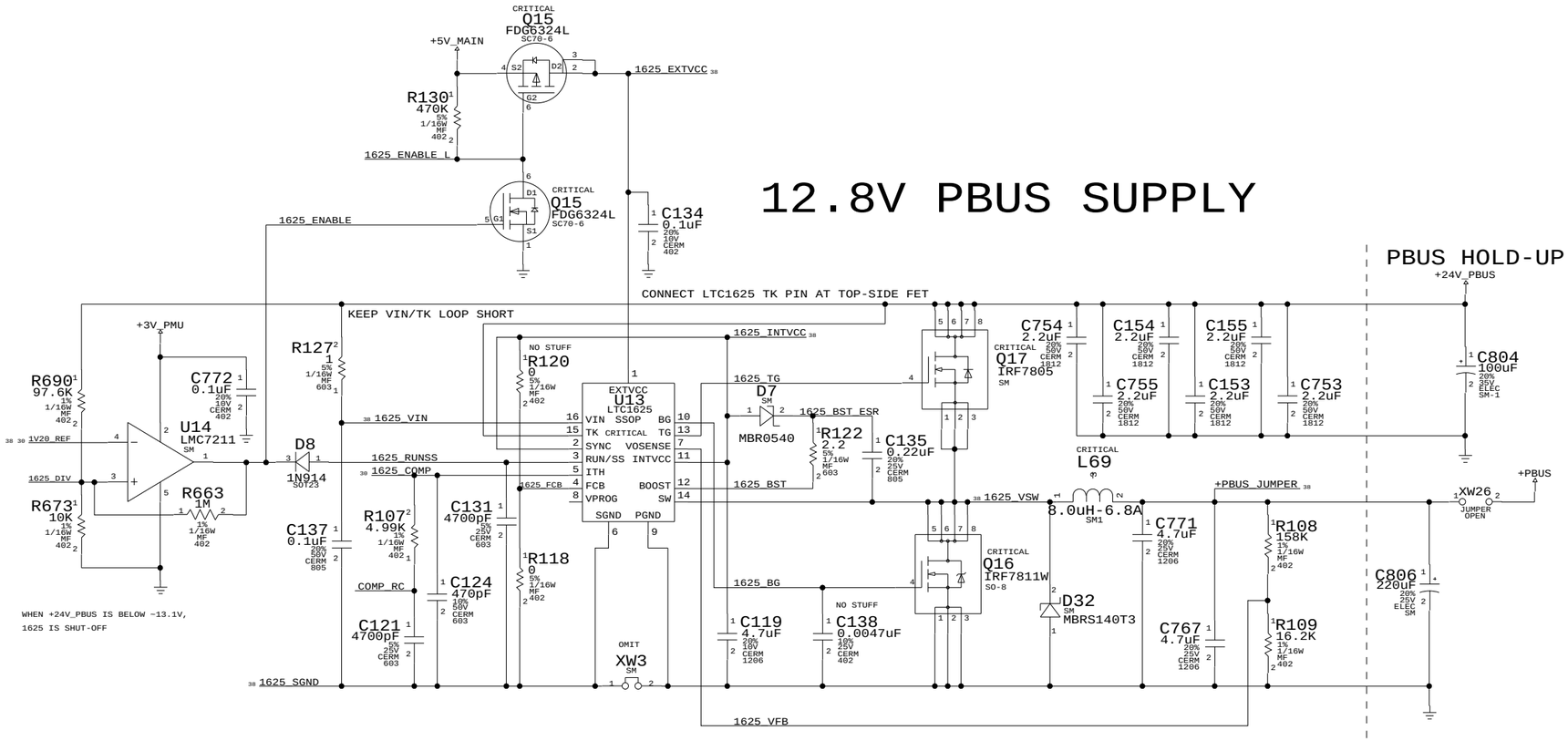
SIZE	DRAWING NUMBER	REV.
D	401243	0A
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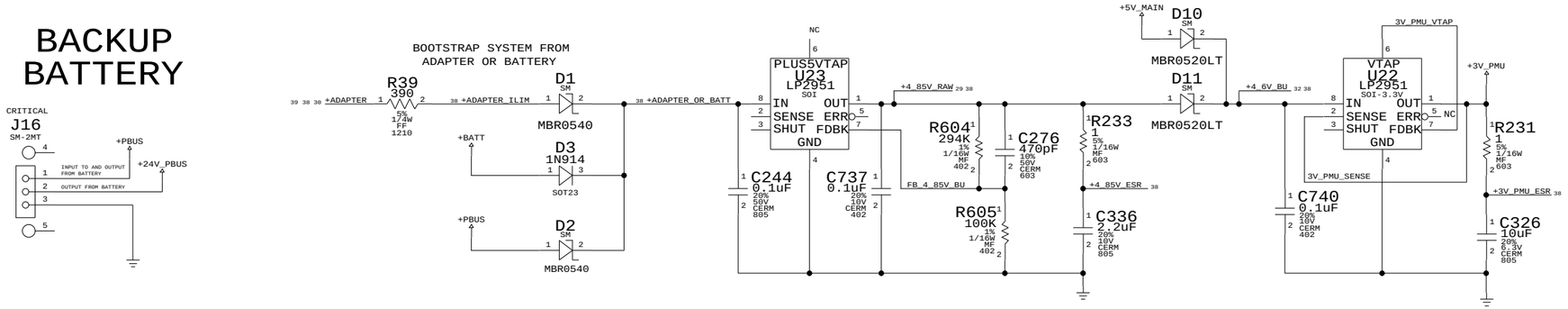


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12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY

12.8V REGULATOR

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3.3V/5V MAIN SUPPLY

DISTRIBUTE CAPS ALONG TOP EDGE AND FAN CUT-OUT

5V START TO TURN ON ~12.5MS AFTER DCDC_EN_L

3V START TO TURN ON ~25MS AFTER DCDC_EN_L

DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN

POWERDOWN DELAY IS AROUND 4MS-15.6MS

THIS SIGNAL IS OPEN COLLECTOR TO GND WHEN POWER IS NOT GOOD
220PF IS USED TO QUIET NOISE ON PGOOD ONCE INTERNAL OPEN DRAIN IS DISENGAGED

DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

3.3V/5V REGULATOR

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V->1.025V

1.35V->1.15V 1.33/1.25Ghz
1.225V->1.175V 1.0Ghz
(value without offset)

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0036	126S0035		C51,C52,C77,C78,C91,C92,C111	126S0035 is a slightly longer part

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

Sense resistor R650 may not be needed!

Keep trace fat and short!!

(VCORE=1.385V for EVTB)

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of VCore

Connect MAX1717 GND pin 13
to GND at bottom-side FET

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT
PIN OF 1000uF CAP
CLOSEST TO CPU

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S1825	1	RES,MF,1/16W,182K OHM,1,0402,SMD	R98		CPU_BTR
116S1472	1	RES,MF,1/16W,470 OHM,5,0402,SMD	R97		CPU_BTR
116S1000	1	RES,MF,1/16W,0 OHM,5,0402,SMD	R93		CPU_BTR

Fmax Test Connections

VCORE SUPPLY

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1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M10 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
DDR RAM	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S:500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S:500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S:500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S:500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S:500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S:500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S:500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSED ROUTES MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A0_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A0_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A1_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_A1_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B0_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B0_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B1_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:3000 MIL	SYSCLK_DDRCLK_B1_UF			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0		250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1		250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1		250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0		250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0		250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1		250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1		250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

T231	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 20
T233	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 20
T232	GPU_TMDS_DN<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T234	GPU_TMDS_DP<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T235	GPU_TMDS_DN<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T236	GPU_TMDS_DP<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T238	GPU_TMDS_DN<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20
T237	GPU_TMDS_DP<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 20

T240	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	5	19
T239	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	5	19
T242	SI_TMDS_DN<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T241	SI_TMDS_DP<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T243	SI_TMDS_DN<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T245	SI_TMDS_DP<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T244	SI_TMDS_DN<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19
T246	SI_TMDS_DP<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING	8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

T263	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610		19 20
T265	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
T264	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
T267	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
T266	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::	19 20

T255	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700		19
T256	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
T260	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
T261	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
T262	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::	19

T268	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22 39
T269	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22 39
T271	TMDS_CONN_DN<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T270	TMDS_CONN_DP<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T272	TMDS_CONN_DN<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T273	TMDS_CONN_DP<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T274	TMDS_CONN_DN<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22
T276	TMDS_CONN_DP<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ
AGP BYTES 2-3	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL	6		(250)	8 MIL SPACING		133.0 MHZ
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ
	AGP_SB_STB	L:S:1050 MIL:1450 MIL	6		(350)	8 MIL SPACING		66.00 MHZ
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL	6		(350)	8 MIL SPACING		66.00 MHZ
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL	7					66.00 MHZ
	AGP_STOP_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_PAR	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_REQ_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_GNT_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
	AGP_RBF_L	L:S:1250 MIL:1950 MIL	6					66.00 MHZ
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL			(200)			100.0 MHZ
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHZ
	HD_DIOW_L	L:S:3000 MIL:5200 MIL			(200)			100.0 MHZ
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING	(200)			100.0 MHZ
	HD_DMACK_L	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ
	HD_CS0_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ
	HD_CS1_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ
	HD_DMARQ	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING	(200)			100.0 MHZ
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ
	EIDE_INT	L:S::500 MIL						33.00 MHZ
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		100 MHZ
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		100.0 MHZ
	ENET_LINK_TXD<7..0>	L:S::600						100.0 MHZ
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_LINK_TX_ER	L:S::400 MIL						100.0 MHZ
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_LINK_TX_EN	L:S::400 MIL						100.0 MHZ
	ENET_MDIO	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_MDC	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_COL	L:S:8000 MIL:9000 MIL						100.0 MHZ
	ENET_CRS	L:S:8000 MIL:9000 MIL						100.0 MHZ
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		100 MHZ
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		100 MHZ
	FW_LINK_CNTL<1..0>	L:S:9000:10000						100 MHZ
	FW_PHY_CNTL<1..0>	L:S::300						100 MHZ
	FW_LINK_LREQ	L:S::300 MIL						100.0 MHZ
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						100.0 MHZ
	FW_PINT	L:S:8500 MIL:9500 MIL						100.0 MHZ

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 10 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 10 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5
	TMDS_DN<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
	TMDS_DP<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
	TMDS_DN<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
	TMDS_DP<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
	TMDS_DN<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
	TMDS_DP<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
1239	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
1240	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5
1245	ATI_TMDS_DN<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8
1246	ATI_TMDS_DP<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8
1237	ATI_TMDS_DN<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8
1238	ATI_TMDS_DP<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8
1243	ATI_TMDS_DN<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
1244	ATI_TMDS_DP<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
USB 2.0 Zo = 90	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING	
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.6MIL (TRACE WIDTH)
S = 7MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	1394 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	1357 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1356 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1358 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	1400 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 33 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	1335 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	1346 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1347 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	1348 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	1349 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1350 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	1351 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	1352 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1353 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	1354 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	1355 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	1360 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1361 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	1340 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	1341 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	1332 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	1312 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1345 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	1310 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1316 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1350 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	1315 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14

SIGNAL CONSTRAINTS - PAGE 3

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	401243	0A
SCALE: NONE	SHT 38 OF 44	

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FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.

FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR. FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2 JTAG_ASIC_TMS	TRUE			13 26
	J3 JTAG_ASIC_TDI	TRUE			13
	J1 JTAG_ASIC_TDO_TP	TRUE			26
	J4 JTAG_ASIC_TCK	TRUE			13 26
	J6 JTAG_ASIC_TRST_L	TRUE			13 26
	J5 CPU_CHKSTP_OUT_L	TRUE			5
	J7 CPU_SRESET_L	TRUE			5
	J9 CPU_HRESET_L	TRUE			5 6 7
	J8 JTAG_CPU_TMS	TRUE			5 6
	J10 JTAG_CPU_TDI	TRUE			5 6
	J12 JTAG_CPU_TDO_TP	TRUE			5
	J11 JTAG_CPU_TCK	TRUE			5 6
	J13 JTAG_CPU_TRST_L	TRUE			5 6
	J18 INT_JTAG_TEI	TRUE			13
	J20 INT_TST_MONIN_PD	TRUE			13
	J19 INT_TST_MONOUT_TP	TRUE			13
	J21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15 INT_I2C_CLK0	TRUE			6 11 13 23
	J14 INT_I2C_DATA0	TRUE			6 11 13 23
	J16 INT_I2C_CLK1	TRUE			13 14 25
	J17 INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	J215 +PBUS	TRUE			38
	J216 +24V_PBUS	TRUE			38
	J25 GPU_VCORE	TRUE			19 20 38
	J24 1778_VFB	TRUE			20 38
	J27 CPU_VCORE_SLEEP	TRUE			5 33 38
	J26 VCORE_FB	TRUE			33 38
	J217 +1_8V_MAIN	TRUE			38
	J218 +2_5V_MAIN	TRUE			38
	J219 +5V_MAIN	TRUE	2		38 39
	J220 +5V_SLEEP	TRUE	2		38 39
	J221 +3V_MAIN	TRUE	4		23 38
		TRUE		1000	→ IN
	J222 +3V_PMU	TRUE			38
CARDBUS	J36 CBUS_DET_1_L	TRUE		2000	18
DVI	J35 CBUS_DET_2_L	TRUE		2000	18
	J37 TMDS_DN<0..2>	TRUE		1000	19 22 37
	J38 TMDS_DP<0..2>	TRUE		1000	19 22 37
	J40 TMDS_CONN_CLKN	TRUE		1000	22 36
	J39 TMDS_CONN_CLKP	TRUE		1000	22 36
	J42 VGA_R	TRUE		1000	22
	J41 VGA_G	TRUE		1000	22
	J44 VGA_B	TRUE		1000	22
	J43 VGA_HSYNC	TRUE		1000	22
	J46 VGA_VSYNC	TRUE		1000	22
	J45 DVI_DDC_CLK_UF	TRUE		1000	22
	J47 DVI_DDC_DATA_UF	TRUE		1000	22
	J48 DVI_HPD_UF	TRUE		1000	22
	J49 +5V_DDC_SLEEP	TRUE		2000	22 38
		TRUE	2	2000	→ IN
CHGND1		TRUE	6	1000	→ IN
LVDS	J52 LVDS_L0N	TRUE		1000	20 22 37
	J51 LVDS_L0P	TRUE		1000	20 22 37
	J53 LVDS_L1N	TRUE		1000	20 22 37
	J55 LVDS_L1P	TRUE		1000	20 22 37
	J54 LVDS_L2N	TRUE		1000	20 22 37
	J57 LVDS_L2P	TRUE		1000	20 22 37
	J56 CLKLVDS_LN	TRUE		1000	20 22 37
	J58 CLKLVDS_LP	TRUE		1000	20 22 37
	J59 LVDS_DDC_CLK	TRUE		1000	20 22
	J60 LVDS_DDC_DATA	TRUE		1000	20 22
	J62 +3V_LCD	TRUE	2	2000	22 38
	J223 +3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	→ IN
CHGND4		TRUE	6	1000	→ IN
INVERTER	J67 +14V_INV	TRUE		2000	22 38
	J66 +5V_INV_SW	TRUE		2000	22 38
	J68 BRIGHT_PWM	TRUE		2000	22
	J249 INV_GND	TRUE		2000	22
		TRUE		1000	→ IN
S-VIDEO	J70 TV_C	TRUE		2000	22
	J72 TV_Y	TRUE		2000	22
	J71 TV_COMP	TRUE		2000	22
	J73 TV_GND1	TRUE		2000	22 38
	J74 TV_GND2	TRUE		2000	22 38
LIO	J76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	J75 INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	J78 INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	J83 INT_I2S0_SND_SCLK	TRUE		1000	14 25
	J82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	J77 SND_HP_MUTE_L	TRUE		1000	14 25
	J79 SND_AMP_MUTE	TRUE		1000	25
	J84 SND_HW_RESET_L	TRUE		1000	14 25
	J85 SND_HP_SENSE_L	TRUE		1000	14 25
	J86 SND_LIN_SENSE_L	TRUE		1000	14 25
	J81 INT_I2C_CLK2	TRUE		1000	14 25
	J80 INT_I2C_DATA2	TRUE		1000	14 25
	J87 ADAPTER_DET	TRUE		1000	25 29
	J88 CHARGE_LED_L	TRUE		1000	25 29
	J89 NEC_LUSB_OCI_UF	TRUE		1000	17 25
	J90 NEC_LUSB_PPON	TRUE		1000	17 25
	J224 +5V_MAIN	TRUE	2	2000	38 39
	J221 +5V_SLEEP	TRUE	2	3000	38 39
	J225 +3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	J94 NEC_USB_DAM	TRUE			17 25 37
	J95 NEC_USB_DAP	TRUE			17 25 37
	J93 NEC_USB_DBM	TRUE			17 25 37
	J97 NEC_USB_DBP	TRUE			17 25 37
	J98 BT_USB_DM	TRUE			14 25 37
	J99 BT_USB_DP	TRUE			14 25 37
	J101 MODEM_USB_DM	TRUE			14 25 37
	J100 MODEM_USB_DP	TRUE			14 25 37
	J102 NEC_RUSB_PPON	TRUE			17 25
	J104 NEC_RUSB_OCI_UF	TRUE			17 25
RT. USB	J105 PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
WIRELESS	J106 PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	J108 PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	J107 PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	J109 PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	J110 PCI_STOP_L	TRUE		1000	12 17 18 24 37
	J111 PCI_PAR	TRUE		1000	12 17 18 24 37
	J112 AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	J113 AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	J114 AIRPORT_PCI_INT_L	TRUE		1000	14 24
	J115 MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	J116 CLK33M_AIRPORT	TRUE		1000	12 24 35
	J118 PMU_PME_L	TRUE		1000	14 17 24 29
	J119 ROM_ONBOARD_CS_L	TRUE		1000	9 24
	J120 ROM_OE_L	TRUE		1000	9 12 24
	J121 ROM_CS_L	TRUE		1000	9 12 24
	J122 ROM_RW_L	TRUE		1000	9 12 24
	J123 RF_DISABLE_L	TRUE		1000	24
	J220 AIRPORT_CLKRUN_L	TRUE		1000	24
	J230 +3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	→ IN
OPTICAL	J126 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	J124 EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	J125 EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	J128 EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	J127 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	J129 EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	J130 EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	J131 EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	J132 EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	J133 EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	J134 EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	J135 +5V_TPAD_SLEEP	TRUE		3000	23 38
	J136 TPAD_F_TXD	TRUE		3000	23
	J137 TPAD_F_RXD	TRUE		3000	23
	J138 LID_CLOSED_L	TRUE		3000	23
	J139 +3V_HALL_EFFECT	TRUE		3000	23 38
	J140 SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/	J141 COMM_RESET_L	TRUE		4000	14 25
SERIAL	J142 COMM_SHUTDOWN	TRUE		4000	14 25
	J143 COMM_RING_DET_L	TRUE		4000	14 25 29
	J144 COMM_TXD_L	TRUE		4000	14 25
	J145 COMM_TRXC	TRUE		4000	14 25
	J146 COMM_GPIO_L	TRUE		4000	14 25
	J147 COMM_DTR_L	TRUE		4000	14 25
	J148 COMM_RTS_L	TRUE		4000	14 25
	J149 COMM_RXD	TRUE		4000	14 25
KEYBOARD	J150 KBD_ID	TRUE		3000	23 29
	J151 KBD_INTL	TRUE		3000	23
	J152 KBD_JIS	TRUE		3000	23
	J153 KBD_CAPSLOCK_LED	TRUE		3000	23
	J154 KBD_NUMLOCK_LED	TRUE		3000	23
	J155 KBD_FUNCTION_L	TRUE		3000	23 29
	J156 KBD_COMMAND_L	TRUE		3000	23 29
	J157 KBD_OPTION_L	TRUE		3000	23 29
	J158 KBD_CONTROL_L	TRUE		3000	23 29
	J159 KBD_SHIFT_L	TRUE		3000	23 29
	J160 KBD_X<0..9>	TRUE		3000	23 29
	J161 KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	J162 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	J163 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	J164 BATT_CLK	TRUE		1000	30
	J165 BATT_DATA	TRUE		1000	30
	J166 PMU_BATT_DET_L	TRUE		1000	29 30
FANS	J167 +FAN_PWR	TRUE		3000	25 38
	J168 FAN1_TACH	TRUE		3000	25
	J169 FAN2_TACH	TRUE		3000	25
	J170 FAN1_GND	TRUE		3000	38
	J171 FAN2_GND	TRUE		3000	38
ETHERNET	J175 MDI_P<0..3>	TRUE		1000	26 37
	J176 MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	J177 FW_TPO0P	TRUE		1000	27 28 37
	J178 FW_TPO0N	TRUE		1000	27 28 37
	J179 FW_TPO0R	TRUE		1000	28
	J179 FW_TPI0P	TRUE		1000	27 28 37
	J180 FW_TPI0N	TRUE		1000	27 28 37
	J181 +FW_VP0	TRUE		1000	28 38
	J182 FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	J183 FW_TPO1P	TRUE		1000	28 37
	J184 FW_TPO1N	TRUE		1000	28 37
	J185 FW_TPI1P	TRUE		1000	28 37
	J186 FW_TPI1N	TRUE		1000	28 37
	J187 +FW_VP1	TRUE		1000	28 38
	J188 FW_VGND	TRUE		1000	39
DC PWR IN	J189 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	J253 ST7_SLEEP_LED_H	TRUE			23
	J250 PMU_SLEEP_LED	TRUE			23
	J251 PMU_LID_CLOSED_L	TRUE			23 29
	J252 LMU_DETECT	TRUE			23
		TRUE	6	1000	→ IN
			(100 MIL PROBE PREFERRED)		
MISC.	J190 SLEEP_LED	TRUE			23
	J191 PMU_KB_RESET_L	TRUE			29
	J192 SLEEP	TRUE			23 25 29 32 34
	J193 PMU_CPU_HRESET_L	TRUE			6 29
	J194 BB_RESET_L	TRUE			6
	J240 +3V_PMU_RESET	TRUE			29 33

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SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 39 OF 44	

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REVISION HISTORY

Proto Release

7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01)
Added P59 SO-DIMM connector as placeholder (p.12)
Added P59 LVDS connector as placeholder (p.22)
Changed J9 to 10 pin Elco connector for modem (p.25)
Changed PBUS holdup caps to P59 electrolytic cans (p.30)

7/23/02 - Removed L3 (p.8)
Replaced processor with 360 pin Apollo (p.5,6)

7/24/02 - Added FETs between battery and PBUS rails for airline power (p.29)

8/10/02 - Added USB 2.0 (p.18)

8/20/02 - Removed spare pullup straps for Intrepid (p.9)
Removed USB overcurrent protection [to be placed on other boards] (p.18)
Changed right USB board connector to 16 pin Hirose connector (p.26)
Changed LIO board connector to 40 pin Molex connector (p.26)
Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)

8/26/02 - Removed 32 bypass caps for +3V_MAIN at Intrepid (p.16)
Removed 5 bypass caps for +2.5V_MAIN at Intrepid (p.16)
Removed 3 bypass caps for +1.5V_AGP at Intrepid (p.16)
Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16)

8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)

8/29/02 - Added dedicated Boot Banger circuit (p.6)
Added 5 bypass caps to each SO-DIMM connector (p.11)
Added quad voltage circuit for bus slewing architecture (p.32)

8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28)
Changed to Q11 adpater detection scheme (p.28)

9/03/02 - Corrected upper LVDS single pin nets (p.20)
Removed unintentional extra pulldown resistor at Intrepid (p.14)

9/17/02 - Numerous changes to stay in sync with P84 (all)

9/18/02 - Changed battery connector back to P84 part (p.29)
Added LMU circuitry to eliminate extra board (p.23)
Changed to P84 dual channel LVDS connector to reduce I2R cable losses(p.22)

9/19/02 - Removed unnecessary battery FETs [due to 3S only design] (p.29)
Modified chassis gnds on some components (all)
Removed LMU connector (p.23)
Corrected battery connector [same as P84] (p.29)
Removed P93 support (p.25)
Removed second fuse from FW ports [single fuse provides adequate power] (p.27)

9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26)
Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)

9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34)
Swapped pins on L33, L35 for layout (p.31)
Changed Y6 to smaller form-factor crystal (p.26)

9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29)
Corrected holes and chassis gnds (p.4,all)

10/01/02 - Removed Intrepid 1.x specific circuitry (p.13)
10/03/02 - Numerous pin-swaps to accomodate board layout (all)
10/08/02 - Added page for functional test points (p.37)
10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23)
10/10/02 - Clamped NEC NC pins high per documentation (p.17)
Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14)
Added R5CG/NO_R5CG stuffing options for CY28512 circuit (p.14)
Removed CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32)
Removed Zebra 15/18 support per P84 (p.27)
Added second FW port power fuse (p.27)
Removed INT_CPUFB_IN cap per P84 (p.8)
Replaced IRF7822 FETs with IRF7811W in battery charger and 14V PBUS switchers (p.29,30)
Renamed optical interface for consistency (p.24,37)
Corrected PLL_CFG<4> for Apollo 7 (needs to always be zero) (p.5,7)
Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
Added stuffing options to power fans off 3V or 5V (p.25)

10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)

10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26)

10/15/02 - Moved Firewire connectors and port power switch to separate page (p.28)
Changed SMBus pullups to 7.15K, 1% as per iBooks/P84 [involved component net swaps] (p.29)
Added 0603 resistors as shorting pads for power up and reset (p.23)
Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14)
Added damping resistor option to LMU crystal (p.23)
Changed INT_TST_PLLEN_PD to pulldown only [LA_clk not used] (p.13)
Changed JTAG_ENET_TDI to pullup [LA_clk not used] (p.13)
Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14)
Changed BBANG_HRESET_L pullup to 3V_SLEEP (p.6)
Changed FW_PC_PD, FW_PC_PU resistors to 5% (p.27)
Added 1K pulldown and net FW_PD2 to FW_PHY (p.27)

10/16/02 - Implemented new FW power switch and current limit (p.28)
Renamed +14V_PBUS to +PBUS (p.all)
Added A29 adapter detection circuit (p.29)
Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30)
Changed FW_PHY_pin DS1 to pullup to make Port 1 1394a only (p.27)

10/21/02 - Updated CY28512 clock chip to Rev B (p.14)
Changed keyboard ZIF to large SMK connector (p.23)
Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7)

10/22/02 - Mirrored wireless connector for P50 flex (p.24)

10/23/02 - Changed LMU/sleep LED interface per p84 (p.23)
Changed LMU JTAG/I2C pinout/pullup/pulldown strategy per P84 (p.23)
Changed fan FETs to SI3446DV per P84 (p.25)
Pinned out audio connector (p.25)
Pinned out right USB connector (p.25)
Pinned out modem connector (p.25)
Added 2 functional test points to wireless connector (p.24,38)
Renamed FW_low_voltage power rails (p.27,37)
Renamed Vcore VID nets to be consistent with P84 (p.33)
Removed redundancy in DDR memory constraints (p.35)

10/24/02 - Changed FW_DS2 strap to pullup in order to port 2 (p.27)
Cleaned up CY28512B circuit as per P84 (powered off main, output divider and strap tweaks) (p.14)
Updated PCI clock series R values per P84 (p.12)
Changed power rail for ALS to +3V_MAIN per P84 (p.23)
Added 0 ohm short and bypass cap for GPU_VDDQV per P84 (p.21,37)
Split FW_VDN0 into FW_VGND0 and FW_VGND1 (p.28,37)
Added TP nets to GPU for XOR-tree testing (p.19-21)
Changed fan PWM output pullups to +3V_SLEEP to prevent pump-up (p.25)

10/28/02 - Added FW thermal pad ground hole back in (p.27)
Repinned LMU pulldown for layout (p.23)

10/30/02 - Changed fan power rails to common net (p.25)

10/31/02 - Removed MLB ALS (p.23)
Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24)

11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5)
Broke out quad OR-gate to discrete components for better placement (p.22,29)

11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28)
Added 3 decoupling caps to CPU_VCORE_SLEEP (p.5)
Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32)
Removed XW19 jumper for CPU_VCORE_SLEEP (p.33)
Added decoupling cap to PMU reset OR gates (p.29)

11/08/02 - Changed Firewire PHY to Z17 (p.27)
Added bulk caps to fan connectors (p.25)

11/11/02 - Added alternate chassis gnd connection for sleep LED (p.23)

11/13/02 - Removed +3V_MAIN option for P50 card (p.24)

11/13/02 - Removed LMU and associated circuitry (p.23)

11/21/02 - Implemented D3cold for all PCI devices (p.12,14,18)

11/25/02 - Renamed all components (all pages)

11/26/02 - Removed chokes from 1394b data pairs (p.27,28)

EVT RELEASE

12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12)
Replaced ADM1031 with ADT7460 [I2C Address Change!] (p.25)
Added ADT7460 hookups to GPU thermal diode (p.21,25)
Added FireWire 8 ESD protection circuits (p.28)

12/16/02 - Removed hole from FireWire ground pad (p.27)
DDR memory connector renamed to J25 (p.11)

12/20/02 - Removed LT4210 from FireWire port power (p.28)
Added F10,F29 as placeholders and experiment guides (p.28)
Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27)

12/26/02 - Updated CPU p/ns to production p/ns (p.5)
Removed RC glitch filter on CPU_DRDY_L (p.5,36)
Updated PCI source clock and internal spreading straps (p.8)
Changed BootROM PWD signal to INT_RESET_L per P84 (p.9)
Added CKE pulldowns per P84 (p.9)
Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13)
Updated SSCG/NO_SSCG BOM options (p.14)
Renamed line-in and headphone sense lines to reflect active low signals (p.14,25.39)
Added 0 ohm Rs to make 2.5V_INTREPID rail hot or cold (p.15,16,38)
10 BUFFed ERCIFIC 1.5V LDO circuit (p.15)
Stuffed USB OC1/PD filters for 8 time constant due to new port current limiters) (p.17)
Renamed USB OC1/PPON signals for left/right ports (p.17,39)
Updated GPU VCore to stay in sync with P84 [jitter improvement] (p.20)
Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25)
Added R800,R801 for eventual thermal diode in CPU (p.25)
Renamed R2009 to R799, R2001 to R802, R2002 to R803 (p.25)
Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28)
Added caps to FW ESD circuit that were missed (p.28)
Changed MAX4172 power source to save current on battery [per P84] (p.30)
Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34)
Replaced all 132S1061 [1uF,0805,10V,20%] with 132S0046 [1uF,0603,10V,20%] (p.14,15,27,30,33,34)
Replaced all 138S0351 [1uF,0603,6.3V,10%] with 132S0046 [1uF,0603,10V,20%] (p.27,30)

01/02/03 - Updated FireWire fuse topology to that of P84 (p.28)
Updated system and power block diagrams (p.2,3)

01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10)

01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11)

01/08/03 - Added 2N7002 circuits to ensure speakers are muted during power-up (p.25)
Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8)

01/09/03 - Added required pulldown to output of DVI HPD sense comparator (p.22)
Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28)
Updated S-video filter values to those of P84 (p.22)

01/10/03 - Z77,Z723,Z761,Z776,Z789,Z787,Z722,Z738,Z760,Z742 & Z717 are changed to HOLE-VIA-20R10 (p.4)

01/13/03 - Add L53, L54, L55 for TMDS Data<0:2> Diff Pair (p.22)

01/14/03 - Add C812 - C821 (Totol 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16)
Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Add R810 & R811 for ALWAYS-ON FANs in Acrylic Build (p.25)

01/28/03 - Remove NV37/17 components (p.19-21)
Add M10 (p.19-21)

02/07/03 - Add Power Net Constraints for M10 (p.38)
Replace Singing PBus Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 12G30035 (for alt. 12G50036) (p.33)

02/11/03 - Add FW Power Net Constraints (p.36)
Change signal constraints for AGP signals (p.36)
Add LMU connector and components (p.23)
Edit I2C table for LMU (p.13)
Change R580 to 19.6K (p.14)
Connect Clock Slewing RESET# to MAIN_RESET_L (p.14)
Change Ferrite Bean of ATI power supply to correct values (p.21)
Remove C141 PBUS CAP (p.31)

02/12/03 - Change and Rotate Keyboard Connector (p.23)
Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)

EVT RELEASE (continue)

02/13/03 - Add C825 (p.30)

02/17/03 - Rename all Reference Designators

EVT ENCLOSURE RELEASE

03/13/03 - Change 3-P FAN connectors to 4-P (p.25)
Add PU at PMU_SLEEP_LED_L for LMU (p.23)
Change stuffing option for clock slewing & PLL5 (p.14)
Change ATI M10 GPIO8 to Pull-down (p.20)
Remove Memory MUX 0ohm Resistors (p.10)

03/28/03 - Due to MLB outline change at DVI connector, CHGND1 has to be splitted into
CHGND1 & CHGND2 (P 4 & 22)
Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32)
R603 change from 100K to 4.7K (P 29)
Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31)
Add C826 at U3 RS- pin (P 30)
Change D3 to 1N914 PN Junction Diode(P 31)

03/31/03 - Change AGPTEST Pull-up to 47ohm (it was 40ohm) (P 20)
Add circuits to prevent start-up Headphone POP (P 25)
Change all 1210 4.7uF to 1206 4.7uF Cap (138S0031) (various pages)
Modify FAN circuit to PWM active low signal (P25)

04/08/03 - Add SOFT_MODEM_support (P 14 & 25)
Add 10-Pin ELCO connector for Serial Debug Interface (P 25)
Change Q7 from SI4435DY to SUD45P03-10 (P 30)
Remove D34 RS3AB (P 30)

04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28)
Change PBUS L69 and VCORE L71 Inductor (P 31 & 33)
Change C643 10uF Cap to 1206 package part (P 28)
Change all 6 VCORE Caps to 220uF Al Poly Cap 128S0024 (P 33)
Add Mitsumi MM1571J regulator to provide 1.8V TPVDD (P 21)
Change U34 to Mitsumi MM1571J part for ATI PLL 1.8V rail(P 21)

04/16/03 - Add FW Port ShutDown/PowerOn Circuit (P 28)
Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)

04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)

04/21/03 - Add 12 ICT JTAG TEST PADs (P 39)

04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20)
Combine Q35 and Q36 into a Dual Package Part (P 22)
SWAP the ADT7460 Temperature Sense pair (P 25)
Change FW PHY to production part (P 26)

04/24/03 - Remove +3V_CBUS_SLEEP and US, use +3V_SLEEP directly (P 14,18,24)
Add 0402 Res between ATI PVDD/TPVDD rail and 10uF caps for stability purpose (P 21)
Add 90ohm common mode choke at TMDS data <0..2> pairs (P 22)
Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)

04/25/03 - Change C826 to 0.01uF 50V Cap (P 30)

04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)

05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)

DVT RELEASE

05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (P.31)

05/27/03 - Change R931 to 4.7K for I2C timing specification (P.13)
Change Q62 & Q65 to SI7308DP part (P.33)
Change Q60, Q63 & Q66 to IRF7832 part and split C102 into 3 10pF caps (P.33)
Enable Vcore Burst(Skip) Mode by no stuffing R67 (P.33)
Enable 3V/5V Burst Mode by changing R406 & R407 to 100K ohm (P.32)
Change Q48 to SI7090DP part (P.20)
Change Q49 to IRF7832 part (P.20)
Enable GPUcore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (P.20)
Reduce audible noise by changing L64 to 152S0139 (P.20)
Add C838, C840, C839, C844 & C845 10pF caps near the power switchers FETs (P.20, 32 & 34)
Change PWM_L_Fan input (both L&R Fans) to +5V_SLEEP pull-up (P.25)

05/30/03 - Connect SLEEP_LED_DGND to digital ground instead of CHGNDS (P.23)

06/03/03 - Add CPU Core Voltage offset option circuit (P.33)
GPU Vcore on/off timing (P.20)

06/05/03 - Change FW-B connector to 514S0058 with internal shield pins (P.28)

06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (P.38)
Change the +2.5V_Sleep FET to reduce Voltage drop on the rail (P.34)

06/12/03 - Change CBUS & USB2_REQ_LINE Pullup to +3V_MAIN (P.12)
Add 0 ohm at USB AVSS_GND (P.17)
Change TMDS common mode choke to TDK AMC2012-900H part (P.22)
Change HD_DMACK_L pullup R213 to 10K (P.24)
Add C847, C851 & C852 at ENET CLK for EMC (P.13 & 26)
Change Q34 to FDS3672 (P.28)
Change Q82 pin#4 connection to system digital GND (P.33)
Add C848 150uF cap at J3 for +5V_MAIN USB2 power (P.25)
Add C853 1000pF cap at Q64 (P.30)
Add RC at ADT7460 power rail for noise isolation (P.25)
Isolate THERM# signal at ADT7460 by using double inverters for THERM_L_OC (P.25)
Remove redundant pullup R681 for THERM_L_OC (P.29)
Remove SH2 EMI spring at CHGNDS (P.23)
Add additional PWR/GND pins at J17 for R-USB board (P.25)

06/13/03 - New SODIMM connector with 4 through-hole mounting pins (P.11)
Change CPU config stuffing option at R63 and R64 (P.7)
Stuff R288 for Cypress clk chip (P.14)
Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (P.12)
Change the TMDS Termination Resistor values to 162ohm (P.20)
Connect C847 at R160.1 (P.13)
Add 1000pF caps at ADT7460 D_plus/minus pairs (P.25)
Add SI1182 DVI transmitter to prevent leakage from DVI connector to the system (P.19&20)

06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (P.20&32)
Remove R271 0ohm resistor (P.34)
Edit Signal Constraints for TMDS routing and ENET routing (P.36&37)

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL      26D2< 38B3>
+1_5V_AGP          12B5< 12D1< 12D4< 15D5< 16C8<
                 19C6< 19D6< 20A8< 20B4<> 20D5<>
                 21B8< 21D6< 38C3>
+1_5V_AGP_GPU      21C5< 38C3>
+1_5V_AGP_NECK     20B4<> 38B3>
+1_5V_GPU_VDD15    20D3< 38C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1_5V_INTREPID_PLL1  14C3< 38D3>
+1_5V_INTREPID_PLL2  14D3< 38D3>
+1_5V_INTREPID_PLL3  14D3< 38D3>
+1_5V_INTREPID_PLL4  14D3< 38D3>
+1_5V_INTREPID_PLL5  12D3< 38D3>
+1_5V_INTREPID_PLL6  12D6< 38D3>
+1_5V_INTREPID_PLL7  8D5< 38D3>
+1_5V_INTREPID_PLL8  14D3< 38C3>
+1_5V_LDO          38D6>
+1_5V_MAIN         38D6>
+1_5V_SLEEP        38D6>
+1_5V_SLEEP_NECK  34D2<> 38B3>
+1_5V_SLEEP_VIN  38D6>
+1_8V_ATI_PVDD     20C5<> 21B6< 21B6< 21D6<> 38C3>
+1_8V_ATI_TPVDD  21D1<> 38B3>
+1_8V_GPU          19A8< 19C2< 20D7< 21A2< 21A6<
                 21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD     21D5< 38B3>
+1_8V_GPU_AVDDQ  21D4< 21D7< 38B3>
+1_8V_GPU_DVO      21B2<
+1_8V_GPU_MEMPLL  21B5< 38B3>
+1_8V_GPU_PLL      21D5< 38C3>
+1_8V_GPU_PNLIO  21A5< 38B3>
+1_8V_GPU_PNLPLL  21B5< 38B3>
+1_8V_GPU_TP_PLL  21B5< 21D1< 38B3>
+1_8V_GPU_VDDDI  21C7< 21D4< 38C3>
+1_8V_MAIN         38D6> 39C6>
+1_8V_PVDD_NECK  20B5<> 38B3>
+1_8V_SLEEP        38D6>
+1_8V_SLEEP_NECK  34D2<> 38B3>
+1_95V_FW_DVDD     27C4< 27C7<> 27D5< 38A3>
+1_95V_FW_DVDD_PORT1  27D6< 38A3>
+1_95V_FW_DVDD_RX0  27C5< 38A3>
+1_95V_FW_DVDD_TX0  27C5< 38A3>
+1_95V_FW_PLL400VDD  27C4< 38A3>
+1_95V_FW_PLL500VDD  27D4< 38A3>
+1_95V_FW_PLLVDD  27D4< 27D6<> 38A3>
+2_5V_CG_MAIN     14C6<
+2_5V_GPU          21A7<> 21B6< 21C6< 21C8< 21D8<
                 38C3>
+2_5V_GPU_A2VDD  21D4< 21D7< 38B3>
+2_5V_GPU_MCLK   21C7< 21D4< 38B3>
+2_5V_GPU_MEMCORE  21C5< 38C3>
+2_5V_GPU_PNLIO  21A5< 38C3>
+2_5V_INTREPID    9A7< 10D3< 10D5< 10D6< 10D8< 15D6<
                 16B8< 38D3>
+2_5V_MAIN         38D6> 39C6>
+2_5V_MARVELL      26B8< 26C4<> 38B3>
+2_5V_MARVELL_AVDD  26C4< 38B3>
+2_5V_SLEEP        38D6>
+2_5V_SLEEP_NECK1  20C4<> 38B3>
+2_5V_SLEEP_NECK2  34D2<> 38B3>
+3V_AIRPORT        38C3> 39C3>
+3V_ATI_OSC_SLEEP  19B2< 38B3>
+3V_ATI_SS         19A3< 38B3>
+3V_CG_PLL_MAIN  14C6<
+3V_FW             27A3< 27D7<> 28D5< 38A3>
+3V_FW_AVDD        27C6< 38A3>
+3V_FW_AVDD_PORT0  27C6< 38A3>
+3V_FW_AVDD_PORT1  27C6< 38A3>
+3V_FW_AVDD_PORT2  27D6< 38A3>
+3V_FW_ESD         28B4<> 28D3<>
+3V_FW_ESD_ILIM  28D4<
+3V_FW_UF          27D7<> 38A3>
+3V_GPU            12D1< 19B8< 19C6< 19C8< 19D6<
                 20C4< 20C5< 20C7< 20D7< 21A6< 21B1<
                 38C3>
+3V_GPU_FLT        21B2< 38C3>
+3V_HALL_EFFECT  23B4<> 38B6> 39B3>
+3V_INTREPID_USB  14C3< 38D3>
+3V_LCD            22B4<> 38B6> 39B6>
+3V_LCD_SW         22B4<> 38B6>
+3V_MAIN           23B7<> 38D6> 39C6>
+3V_MAIN_AUD       25C6<> 32C1<> 38B6>
+3V_MAIN_JUMPER  32D2<> 38D1>
+3V_NEC_VDD        17B3< 17D7< 17D7< 38A3>
+3V_PMU            38D6> 39C6>
+3V_PMU_AVCC       25B1< 29B6< 29D5<> 38C6>
+3V_PMU_ESR        31A2< 38C6>
+3V_PMU_RESET      29B7< 33A4<> 39C1>
+3V_SI_AVCC        19D3<
+3V_SI_PLLVCC      19D3<
+3V_SI_VCC         19D3<
+3V_SLEEP          38D6> 39A6> 39B6>
+3V_SLEEP_NECK     34D1<> 38B3>
+3V_SLP_OK_L       32B4<>
+3V_SLP_ON         32A5<>
+4_6V_BU           31B3<> 32B7< 38C6>
+4_85V_ESR         31A4< 38C6>
+4_85V_RAW         29A5< 31B4<> 38C6>
+5V_DDC_SLEEP      22D3<> 22D5<> 38B6> 39B6>
+5V_DDC_SLEEP_UF  22D6< 38B6>
+5V_HD_SLEEP       24D1<> 32A7<> 38C6>
+5V_INV_SW         22B2<> 38B6> 39A6>
+5V_INV_UF_SW      22B2<> 38B6>
+5V_MAIN           38D6> 39A6> 39C6>
+5V_MAIN_AUD       25C6<> 32C8<> 38B6>
+5V_MAIN_JUMPER  32D8<> 38D1>
+5V_SLEEP          38D6> 39A6> 39C6>
+5V_TPAD_SLEEP     23B5<> 38B6> 39B3>
+14V_INV           22B2<> 38B6> 39B6>
+24V_PBUS          38D6> 39C6>
+ADAPTER           30D8<> 31A7< 38C6> 39D1>
+ADAPTER_ILIM      31A6<> 38C6>
+ADAPTER_OR_BATT  31A5<> 38C6>
+ADAPTER_SENSE     30D4<> 38C6>
+ADAPTER_SW        30D5<> 38C6> 38C6>
+BATT              38D6>
+BATT_14V_FUSE     30D1<> 38C6>
+BATT_24V_FUSE     30B1< 30D2<> 38C6>
+BATT_POS          30A4<> 38C6> 39A3>
+BATT_RSNS         30B2< 38C6>
+BATT_VSNS         30A4< 38C6>
+FAN_PWR           25A3< 25A4< 38B6> 39A3>
+FW_AMP_SENSE      28D6<> 38A3>
+FW_PBUS           28D8<> 38A3>
+FW_PWR1           28C5< 38A3>
+FW_PWR_OR         27B8< 27D8<> 28D5<> 38A3>
+FW_SW             28D5<> 38A3>
+FW_VP0            28C1<> 38A3> 39A3>
+FW_VP1            28A3<> 38A3> 39D1>
+GPU_VDD15_NECK  20B5<> 38B3>
+GPU_VDD15_UF      20B5<> 20D4<> 38B3>
+HD_LOGIC_SLEEP  24C2<> 38C6>
+PBUS              38D6> 39C6>
+PBUS_JUMPER       31C3<> 38D1>
+VCC_CBUS_SW       18B1< 18B2<> 18D2<> 38C3>
+VPP_CBUS_SW       18B1< 18B2<> 18D2<> 38C3>
1V20_REF           30C7< 31C8< 38D1>
1V65_REF           30A5<
1_5V_BOOST         34C6<> 38C1>
1_5V_BST           34C5<> 38C1>
1_5V_DH            34C5<> 38C1>
1_5V_DL            34B5<> 38C1>
1_5V_FB            34B5< 34B7< 38C1>
1_5V_ILIM          34C5<> 38C1>
1_5V_LX            34B5<> 38C1>
1_5V_LX_F          34B7<> 34C5> 38C1>
1_5V_SLEEP_EN_L  34C7<> 34D7<>
1_8V_PVDD_STD      21D6<
1_8V_SLEEP_PWREN_L  34A3<>
1_8V_SW            34A5<> 38A1>
1_8V_SW_F          34A4<> 38A1>
1_8V_TPVDD_STD     21D1<
1_8V_VFB           34A5<> 38A1>
2_5V_BOOST         34C4<> 38D1>
2_5V_BST           34C4<> 38D1>
2_5V_DH            34C4<> 38D1>
2_5V_DL            34B4<> 38C1>
2_5V_ILIM          34C5<> 38C1>
2_5V_LX            34B4<> 38D1>
2_5V_LX_F          34B2<> 34C4> 38D1>
2_5V_SLEEP_PWREN_L  34C2<>
3V_5V_OK           32B4<> 34A8< 34D6<
3V_BG              32C4<>
3V_BOOST           32C4<>
3V_BOOST_ESR       32D3<>
3V_ITH             32C4<>

3V_ITH_RC          32C3<
3V_PMU_VTAP        31B3<
3V_RSNS            32D2< 38D1>
3V_RUNSS           32C4<
3V_SLEEP_PWREN_L  32B3<>
3V_SNSM            32C4< 37A2>
3V_SNSP            32C4< 37A2>
3V_SW              32C4<> 38D1>
3V_TG              32D4<>
3V_VOSNS           32C4<>
5V_BG              32C5<>
5V_BOOST           32C5<>
5V_BOOST_ESR       32D6<>
5V_HD_PWREN        32A8<>
5V_ITH             32C5<>
5V_ITH_RC          32C6<
5V_RSNS            32D7< 38D1>
5V_RUNSS           32C5<
5V_SLEEP_PWREN     32A8<>
5V_SNSM            32C5< 37A2>
5V_SNSP            32C5< 37A2>
5V_SW              32C5<> 38D1>
5V_TG              32C5<>
5V_VOSNS           32C5<>
1625_BG            31C5<>
1625_BST           31C5<
1625_BST_ESR       31C5<>
1625_COMP          30D2< 31C6<
1625_DIV           31C8<
1625_ENABLE        31D7<>
1625_ENABLE_L      31D6<>
1625_EXTVCC        31D5<> 38D1>
1625_FCB           31C6<
1625_INTVCC        31C5<> 38D1>
1625_RUNSS         31C6<
1625_SGND          31B7<> 38D1>
1625_TG            31C5<>
1625_VFB           31B5<>
1625_VIN           31C6< 38D1>
1625_VSW           31C4<> 38D1>
1772_ACIN          30B5<
1772_ACOK_L        30B5<> 30C4<>
1772_BST           30B4<>
1772_BST_ESR       30C3<
1772_CCI           30B5<>
1772_CCS           30B5<
1772_CCV           30B5<>
1772_CCV_RC        30B5<
1772_CELLS         30B4<
1772_CLS           30A4<
1772_CSIN          30B4<> 37A2>
1772_CSIP          30B4<> 37A2>
1772_CSSN          30C5< 37A2>
1772_CSSP          30C5< 37A2>
1772_DCIN          30B5<> 38C6>
1772_DHI           30B4<>
1772_DLO           30B4<>
1772_DLOV          30B4<> 38C6>
1772_GND           30A5<> 38C6>
1772_ICHG          30B5<>
1772_ICTL          30B5<>
1772_IINP          30B5<
1772_LDO           30C4<> 38C6>
1772_LX            30B4<> 38C6>
1772_REF           30B5<>
1772_VCTL          30B5<
1778_BG            20A5<> 38B1>
1778_BST           20A5<> 38B1>
1778_BST_RC        20A5< 38B1>
1778_FCB           20A6< 38B1>
1778_GND           20A6< 20A7<> 38B1>
1778_ION           20A5< 38B1>
1778_ITH           20A6<> 38B1>
1778_ITH_RC        20A7< 38B1>
1778_SHDN_L        20A6<>
1778_TG            20A5<> 38B1>
1778_VCC           20A5< 38B1>
1778_VFB           20A2< 20A5< 38B1> 39C6>
1778_VIN           20A5< 38B1>
1778_VRNG          20A6< 38B1>
3405_MODE          26D5<
3405_VFB           26D4<>
3707_FCB           32C5<
3707_FSET          32C5<
3707_INTVCC        32D4<> 38D1>
3707_SGND          32B5<> 38D1>
3707_STBY          32C5<>
A29_CLS_ADJ        30A5<>
A29_CURRENT_ADJ  30C4<>
A29_DETECT         29A2< 30A5<> 30C4<>
A29_DET_L          29A3<
A29_DET_REF        29A4<
AC_DIV             30C7<
AC_ENABLE_GATE     30D6<>
AC_ENABLE_L        30C5<>
AC_GTR_18V         30C3<>
AC_IN              26B8<> 28C8< 29B3< 30C5<> 30C6<>
AC_IN_FW_CNTL      28C8<>
AC_IN_L            30C2<> 30C6<>
AC_IN_L_RC         30C2<>
ADAPTER_DET        25D8<> 29A4< 39A6>
ADAPTER_I_REG      30D3<>
ADT7460_ADR_ENABLE_L  25B3<>
ADT7460_TACH3_TP  25B3<
ADT7460_THERM_L  25B2<> 25B3<>
ADT7460_VCC        25C4<
ADT7460_VCORE_MON  5C8<> 25B4<>
AGP8X_DET_PU       19C6<>
AGP_AD<0>          12D2<> 19C7<>
AGP_AD<15..0>    37D5>
AGP_AD<1>          12C2<> 19C7<>
AGP_AD<2>          12C2<> 19C7<>
AGP_AD<3>          12C2<> 19C7<>
AGP_AD<4>          12C2<> 19C7<>
AGP_AD<5>          12C2<> 19C7<>
AGP_AD<6>          12C2<> 19C7<>
AGP_AD<7>          12C2<> 19C7<>
AGP_AD<8>          12C2<> 19C7<>
AGP_AD<9>          12C2<> 19C7<>
AGP_AD<10>         12C2<> 19C7<>
AGP_AD<11>         12C2<> 19C7<>
AGP_AD<12>         12C2<> 19C7<>
AGP_AD<13>         12C2<> 19C7<>
AGP_AD<14>         12C2<> 19C7<>
AGP_AD<15>         12C2<> 19C7<>
AGP_AD<16>         12C2<> 19C7<>
AGP_AD<31..16>   37D5>
AGP_AD<17>         12C2<> 19C7<>
AGP_AD<18>         12C2<> 19C7<>
AGP_AD<19>         12C2<> 19C7<>
AGP_AD<20>         12C2<> 19C7<>
AGP_AD<21>         12C2<> 19C7<>
AGP_AD<22>         12C2<> 19C7<>
AGP_AD<23>         12C2<> 19C7<>
AGP_AD<24>         12C2<> 19C7<>
AGP_AD<25>         12C2<> 19C7<>
AGP_AD<26>         12C2<> 19D7<>
AGP_AD<27>         12B2<> 19D7<>
AGP_AD<28>         12B2<> 19D7<>
AGP_AD<29>         12B2<> 19D7<>
AGP_AD<30>         12B2<> 19D7<>
AGP_AD<31>         12B2<> 19D7<>
AGP_AD_STB<0>      12A2<> 12B2< 19D6<> 37D5>
AGP_AD_STB<1>      12A2<> 12B2< 19D6<> 37D5>
AGP_AD_STB_L<0>  12A2<> 12B2< 19D6<> 37D5>
AGP_AD_STB_L<1>  12A2<> 12A2< 19D6<> 37D5>
AGP_ATI_INT_L      14B5<> 19B7<>
AGP_ATI_RESET_L  19B7<
AGP_ATI_VREF       19B7<
AGP_ATI_VREFG      19B7<
AGP_BUSY_L         12C4<> 12D2< 19D6>
AGP_CBE<0>         12B2<> 19B7<>
AGP_CBE<1..0>    37D5>
AGP_CBE<1>         12B2<> 19B7<>
AGP_CBE<2>         12B2<> 19B7<>
AGP_CBE<3..2>    37D5>
AGP_CBE<3>         12B2<> 19B7<>
AGP_DEVSEL_L       12B2<> 12C2< 19B7<> 37D5>
AGP_FRAME_L        12B2<> 12C2< 19B7<> 37D5>
AGP_GNT_L          12C2< 12D2<> 19B7< 37D5>
AGP_IRDY_L         12B2<> 12C2< 19B7<> 37D5>
AGP_PAR            12B2<> 19B7> 37D5>
AGP_PIPE_L         12A2<> 12B2<
AGP_RBF_L          12A2<> 12C2< 19C6> 37C5>
AGP_REQ_L          12C2< 12D2<> 19B7<> 37D5>
AGP_SBA<0>         12B2< 19C6>
AGP_SBA<7..0>    37D5>
AGP_SBA<1>         12B2<> 19C6>

AGP_SBA<2>         12B2<> 19C6>
AGP_SBA<3>         12B2<> 19C6>
AGP_SBA<4>         12B2<> 19C6>
AGP_SBA<5>         12B2<> 19C6>
AGP_SBA<6>         12B2<> 19C6>
AGP_SBA<7>         12B2<> 19C6<>
AGP_SB_STB         12B2<> 12B2< 19C6<> 37D5>
AGP_SB_STB_L       12A2<> 12A2< 19C6<> 37D5>
AGP_ST<0>          12A2<> 19C6<
AGP_ST<1>          12A2<> 19C6<
AGP_ST<2>          12A2<> 19C6<
AGP_STOP_L         12B2<> 12C2< 19B7<> 37D5>
AGP_STP_L          19C6<
AGP_SUS_STAT_L_PU  19C6<
AGP_TRDY_L         12B2<> 12C2< 19B7<> 37D5>
AGP_WBF_L          12A4<> 12B2< 19B7>
AIRPORT_CLKRUN_L  24C6<> 39C3>
AIRPORT_IDSEL      24C5<>
AIRPORT_PCI_GNT_L  12D7<> 24D5<> 39C3>
AIRPORT_PCI_INT_L  14B5<> 14D7< 24D5<> 39C3>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39C3>
ATI_AGP_FBSKEW<0>  20C2< 20C7<>
ATI_AGP_FBSKEW<1>  20C2< 20C7<>
ATI_BUS_CFG<0>   20B2< 20C7<>
ATI_BUS_CFG<1>   20B2< 20C7<>
ATI_BUS_CFG<2>   20B2< 20C7<>
ATI_CLK27M_IN      19A2< 20B7< 35B1>
ATI_CLK27M_OSC     19A2< 35B1>
ATI_CLK27M_OSC_SS  19A1< 19A4< 35B1>
ATI_DBI_HI_PU      19C6<>
ATI_DBI_LO_PU      19C6<>
ATI_DVOD<0>        19B4< 20D7<>
ATI_DVOD<11..0>  36C1>
ATI_DVOD<1>        19B4< 20D7<>
ATI_DVOD<2>        19B4< 20D7<>
ATI_DVOD<3>        19B4< 20D7<>
ATI_DVOD<4>        19B4< 20D7<>
ATI_DVOD<5>        19B4< 20D7<>
ATI_DVOD<6>        19B4< 20D7<>
ATI_DVOD<7>        19B4< 20D7<>
ATI_DVOD<8>        19B3< 20D7<>
ATI_DVOD<9>        19B3< 20D7<>
ATI_DVOD<10>       19B3< 20D7<>
ATI_DVOD<11>       19B3< 20D7<>
ATI_DVOD_DE        19B3< 20C7<> 36C1>
ATI_DVOVMODE       21A3<
ATI_DVO_CLKP       19B3< 20C7<> 36C1>
ATI_DVO_HSYNC      19B3< 20C7<> 36C1>
ATI_DVO_VSYNC      19B3< 20C7<> 36C1>
ATI_GPIO7_SPN      20C7<>
ATI_GPIO8_PD       20C7<>
ATI_GPIO9_SPN      20C7<>
ATI_GPIO10_SPN     20C7<>
ATI_GPIO11_SPN     20C7<>
ATI_GPIO12_SPN     20C7<>
ATI_GPIO13_SPN     20C7<>
ATI_HSYNC          20D5<> 22D8<
ATI_HSYNC_BUF      22D8<>
ATI_MEMTEST        19A6<>
ATI_MEMVMODE0      19A7<
ATI_MEMVMODE1      19A7<
ATI_OSC_OE         19A3<
ATI_PVDD_BYP       21D6<>
ATI_R2SET          20D6<>
ATI_RSET           20D6<>
ATI_RSTB_MSK       19C6<>
ATI_SSCLK_IN       19A2< 20B7<> 35B1>
ATI_SSCLK_UF       19A2<> 35B1>
ATI_TESTEN         20B7<
ATI_TMDS_CLKN      20B7> 20B8< 37B2>
ATI_TMDS_CLKP      20B7> 20B8< 37B2>
ATI_TMDS_DN<0>     20B7> 20B7< 37B2>
ATI_TMDS_DN<1>     20B7> 20B8< 37B2>
ATI_TMDS_DN<2>     20B7> 20B7< 37B2>
ATI_TMDS_DP<0>     20B7> 20B7< 37B2>
ATI_TMDS_DP<1>     20B7> 20B8< 37B2>
ATI_TMDS_DP<2>     20B7> 20B7< 37B2>
ATI_TPVDD_BYP      21D1<>
ATI_VSYNC          20D5<> 22D8<
ATI_VSYNC_BUF      22D8<>
ATI_X1CLK_SKEW<0>  20C2< 20C7<>
ATI_X1CLK_SKEW<1>  20B2< 20C7<>
AUD_GND            25C8<> 38B6>
AUXWIN_PU          20C6<>
BATTV_HIGH         30B7<>
BATTV_LOW          30B8<>
BATT_14PBUS_EN     30C1<>
BATT_14V_GATE      30C1<>
BATT_24PBUS_EN     30C2<>
BATT_24V_GATE      30C1<>
BATT_CLK           30A4<> 39A3>
BATT_DATA          30A4<> 39A3>
BATT_DIV           30A5<
BATT_LOW           30A6<>
BATT_LOW_L         30B6<>
BATT_NEG           30A4<> 38C6> 39A3>
BBANG_HRESET_L     6A2< 6B3<>
BBANG_JTAG_TCK     6A4< 6B2<> 6C2<
BBANG_TCK_EN       6A4<
BB_EEPR_ADDR       6C2< 6D3<
BB_EEPR_WP_PD      6D2<>
BB_MISO            6B3<> 6C2<
BB_MOSI            6B3<> 6C2<
BB_RESET_L         6C3< 39C1>
BB_SCK             6B3<> 6C2<
BB_XTAL1_SPN       6C3<>
BFR_TDO            6C2< 6C2<>
BKFD_PROT_EN_L     30C5<>
BKFD_PROT_GATE     30D5<>
BRIGHT_PWM         22A2<> 39A6>
BRIGHT_PWM_UF      22A2<>
BT_USB_DM          14C1< 25D8<> 37B2> 39D3>
BT_USB_DP          14C1< 25D8<> 37B2> 39D3>
CAPSLOCK_LED       23C2<
CAPSLOCK_LED_L     23C3< 29C7<
CBUS_ADDR<0>       18B1<> 18B4>
CBUS_ADDR<1>       18B1<> 18B4>
CBUS_ADDR<2>       18B1<> 18B4>
CBUS_ADDR<3>       18B1<> 18B4>
CBUS_ADDR<4>       18B1<> 18B4>
CBUS_ADDR<5>       18B1<> 18B4>
CBUS_ADDR<6>       18B1<> 18B4>
CBUS_ADDR<7>       18B1<> 18B4>
CBUS_ADDR<8>       18B1<> 18B4>
CBUS_ADDR<9>       18B1<> 18B4>
CBUS_ADDR<10>      18B4> 18C1<>
CBUS_ADDR<11>      18B1<> 18B4>
CBUS_ADDR<12>      18B1<> 18B4>
CBUS_ADDR<13>      18B1<> 18B4>
CBUS_ADDR<14>      18B1<> 18B4>
CBUS_ADDR<15>      18B1<> 18B4>
CBUS_ADDR<16>      18B1<> 18B4<
CBUS_ADDR<17>      18B2<> 18B4>
CBUS_ADDR<18>      18B2<> 18B4>
CBUS_ADDR<19>      18B2<> 18B4>
CBUS_ADDR<20>      18B2<> 18B4>
CBUS_ADDR<21>      18B2<> 18B4>
CBUS_ADDR<22>      18A4> 18B2<>
CBUS_ADDR<23>      18A4> 18B2<>
CBUS_ADDR<24>      18A4> 18B2<>
CBUS_ADDR<25>      18A4> 18B2<>
CBUS_ADDR_16_UF  18B5<>
CBUS_BVD1_L        18A2<> 18C4<
CBUS_BVD2_L        18B2<> 18C4<
CBUS_CE1_L         18C1<> 18C4>
CBUS_CE2_L         18B2<> 18B4>
CBUS_DATA<0>       18A1<> 18A4<>
CBUS_DATA<1>       18A1<> 18A4<>
CBUS_DATA<2>       18A1<> 18A4<>
CBUS_DATA<3>       18A4<> 18C1<>
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CBUS_DATA<5>       18A4<> 18C1<>
CBUS_DATA<6>       18A4<> 18C1<>
CBUS_DATA<7>       18A4<> 18C1<>
CBUS_DATA<8>       18A2<> 18A4<>
CBUS_DATA<9>       18A2<> 18A4<>
CBUS_DATA<10>      18A2<> 18A4<>
CBUS_DATA<11>      18A4<> 18C2<>
CBUS_DATA<12>      18A4<> 18C2<>
CBUS_DATA<13>      18A4<> 18C2<>
CBUS_DATA<14>      18A4<> 18C2<>
CBUS_DATA<15>      18A4<> 18C2<>
CBUS_DET_1_L       18C2<> 18C4< 39C6>
CBUS_DET_2_L       18A2<> 18C4< 39C6>
CBUS_INPACK_L      18B2<> 18B4<
CBUS_INT_L         14B5<> 14D7< 18A7<>
CBUS_IORD_L        18B2<> 18C4>
CBUS_IOWR_L        18B2<> 18C4>

CBUS_MFUNC1_PD     18A7<> 18A7<
CBUS_MFUNC2_PD     18A7<> 18A7<
CBUS_MFUNC3_PD     18A7<> 18A7<
CBUS_MFUNC4_PD     18A7<> 18A7<
CBUS_MFUNC5_PD     18A7<> 18A7<
CBUS_MFUNC6_PD     18A7<> 18A7<
CBUS_OE_L          18B1<> 18C4<
CBUS_PCI_GNT_L     12D7<> 18A7<
CBUS_PCI_IDSEL     18B7<
CBUS_PCI_REQ_L     12A7< 12D7<> 18A7<
CBUS_PCI_RESET_L  18A7<
CBUS_READY         18B1<> 18C4<
CBUS_REG_L         18B2<> 18C4>
CBUS_RESET_L       18B2<> 18C4>
CBUS_SUSPEND_PU  18A7< 18D7<
CBUS_VCCD0_L       18C4<>
CBUS_VCCD1_L       18C4<>
CBUS_VPPD0         18C4<>
CBUS_VPPD1         18C5<>
CBUS_VS1           18B2<> 18C4<>
CBUS_VS2           18B2<> 18C4<>
CBUS_WAIT_L        18B2<> 18B4<
CBUS_WE_L          18B1<> 18C4>
CBUS_WP_L          18A1<> 18B4<
CG_ADDRSEL         14B7<
CG_CLKOUT          14B6<>
CG_FSEL            14B7< 14C5<>
CG_LOCK            14B7<>
CG_RESET_L         14B7<
CHARGE_DISABLE     30A7<>
CHARGE_LED_L       25D8<> 29C6<> 29D7< 39A6>
CLK10M_PMU_XIN     29B6<
CLK10M_PMU_XOUT  29B6<
CLK10M_PMU_XOUT_UF  29B7<
CLK18M_INT_EXT     14B6<> 35B1>
CLK18M_INT_XIN     14A5< 35B1>
CLK18M_INT_XOUT  14A5<> 35B1>
CLK18M_XTAL_IN     14A5< 35B1>
CLK25M_ENET_XIN  26A7<>
CLK25M_ENET_XOUT  26A7<>
CLK25M_XTAL_IN     26A7<>
CLK32K_PMU_XIN     29B3<>
CLK32K_PMU_XOUT  29B3<>
CLK32K_PMU_XOUT_UF  29B2<>
CLK33M_AIRPORT     12D8< 24D5<> 35C1> 39C3>
CLK33M_AIRPORT_UF  12C7<> 35C1>
CLK33M_CBUS        12D8< 18A7<> 35C1>
CLK33M_CBUS_UF     12C7<> 35C1>
CLK33M_NEC         12C8< 17B7< 35C1>
CLK33M_NEC_UF      12C7<> 35C1>
CLK66M_AGP_1_5V_TP  12C4>
CLK66M_GPU_AGP     12C8< 19B7< 35C1>
CLK66M_GPU_AGP_UF  12C7<> 35C1>
CLKENET_LINK_GBE_REF  13C5< 26C8< 35B1>
CLKENET_LINK_GTX  13C5<> 35A1>
CLKENET_LINK_RX  13D5< 26C8< 35B1>
CLKENET_LINK_TX  13D5< 26D8< 35A1>
CLKENET_PHY_GBE_REF  26C7<> 35B1>
CLKENET_PHY_GTX  13C6< 26C7< 35A1>
CLKENET_PHY_RX     26C7<> 35B1>
CLKENET_PHY_TX     26D7<> 35A1>
CLKFW_LINK_LCLK  13C3<> 35A1>
CLKFW_LINK_PCLK  13C3<> 27C3< 35A1>
CLKFW_PHY_LCLK     13C2< 27B7< 35A1>
CLKFW_PHY_PCLK     27B4> 27C4< 35A1>
CLKLVDS_LN         20B5> 22A4<> 37C2> 39B6>
CLKLVDS_LP         20B5> 22A4<> 37C2> 39B6>
CLKLVDS_UN         20B5> 22A4<> 37C2>
CLKLVDS_UP         20B5> 22A4<> 37C2>
COMM_DTR_L         14C2> 25C1<> 39B3>
COMM_GPIO_L        14C2<> 25C2<> 39B3>
COMM_RESET_L       14C5<> 25D4<> 39B3>
COMM_RING_DET_L  14B5<> 14C7< 25C3<> 29C6<> 39B3>
COMM_RTS_L         14C2> 25C1<> 39B3>
COMM_RXD           14C2<> 25C1<> 39B3>
COMM_SHUTDOWN      14C5<> 25D4<> 39B3>
COMM_TRXC          14C2<> 25C2<> 39B3>
COMM_TXD_L         14C2<> 25C2<> 39B3>
COMP_RC            31C6<
CPU_AACK_L         5A7< 8B5<> 8C2< 36D5>
CPU_ADDR<0>        5C7<> 8D5<>
CPU_ADDR<0..31>  36D5>
CPU_ADDR<1>        5C7<> 8D5<>
CPU_ADDR<2>        5C7<> 8D5<>
CPU_ADDR<3>        5C7<> 8D5<>
CPU_ADDR<4>        5C7<> 8D5<>
CPU_ADDR<5>        5C7<> 8C5<>
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CPU_ADDR<8>        5C7<> 8C5<>
CPU_ADDR<9>        5C7<> 8C5<>
CPU_ADDR<10>       5B7<> 8C5<>
CPU_ADDR<11>       5B7<> 8C5<>
CPU_ADDR<12>       5B7<> 8C5<>
CPU_ADDR<13>       5B7<> 8C5<>
CPU_ADDR<14>       5B7<> 8C5<>
CPU_ADDR<15>       5B7<> 8C5<>
CPU_ADDR<16>       5B7<> 8C5<>
CPU_ADDR<17>       5B7<> 8C5<>
CPU_ADDR<18>       5B7<> 8C5<>
CPU_ADDR<19>       5B7<> 8C5<>
CPU_ADDR<20>       5B7<> 8C5<>
CPU_ADDR<21>       5B7<> 8C5<>
CPU_ADDR<22>       5B7<> 8C5<>
CPU_ADDR<23>       5B7<> 8C5<>
CPU_ADDR<24>       5B7<> 8C5<>
CPU_ADDR<25>       5B7<> 8C5<>
CPU_ADDR<26>       5B7<> 8C5<>
CPU_ADDR<27>       5B7<> 8C5<>
CPU_ADDR<28>       5B7<> 8C5<>
CPU_ADDR<29>       5B7<> 8C5<>
CPU_ADDR<30>       5B7<> 8C5<>
CPU_ADDR<31>       5B7<> 8C5<>
CPU_ARTRY_L        5A7<> 8B5<> 8D2< 36D5>
CPU_AVDD           5C3< 38D3>
CPU_BG_L           5C7< 8C2< 8D5<> 36D5>
CPU_BR_L           5C7> 8D2< 8D5< 36D5>
CPU_BUS_VSEL       5C3< 7A6<
CPU_CHKSTP_OUT_L  5B3<> 5C2< 39D6>
CPU_CHKS_L         5A3< 5D2<
CPU_CI_L           5A7> 8B5<> 36D5>
CPU_CLKOUT_SPN     5C3>
CPU_CLK_EN         8A5< 29C4<>
CPU_DATA<0>        6D8<> 8D3<>
CPU_DATA<0..31>  36D5>
CPU_DATA<1>        6D8<> 8D3<>
CPU_DATA<2>        6D8<> 8D3<>
CPU_DATA<3>        6D8<> 8D3<>
CPU_DATA<4>        6D8<> 8D3<>
CPU_DATA<5>        6D8<> 8D3<>
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CPU_DATA<7>        6D8<> 8D3<>
CPU_DATA<8>        6D8<> 8D3<>
CPU_DATA<9>        6C8<> 8D3<>
CPU_DATA<10>       6C8<> 8D3<>
CPU_DATA<11>       6C8<> 8D3<>
CPU_DATA<12>       6C8<> 8C3<>
CPU_DATA<13>       6C8<> 8C3<>
CPU_DATA<14>       6C8<> 8C3<>
CPU_DATA<15>       6C8<> 8C3<>
CPU_DATA<16>       6C8<> 8C3<>
CPU_DATA<17>       6C8<> 8C3<>
CPU_DATA<18>       6C8<> 8C3<>
CPU_DATA<19>       6C8<> 8C3<>
CPU_DATA<20>       6C8<> 8C3<>
CPU_DATA<21>       6C8<> 8C3<>
CPU_DATA<22>       6C8<> 8C3<>
CPU_DATA<23>       6C8<> 8C3<>
CPU_DATA<24>       6C8<> 8C3<>
CPU_DATA<25>       6C8<> 8C3<>
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CPU_DATA<28>       6C8<> 8C3<>
CPU_DATA<29>       6C8<> 8C3<>
CPU_DATA<30>       6C8<> 8C3<>
CPU_DATA<31>       6C8<> 8C3<>
CPU_DATA<32>       6C8<> 8C3<> 8D8<
CPU_DATA<32..63>  36D5>
CPU_DATA<33>       6C8<> 8C3<> 8D8<
CPU_DATA<34>       6C8<> 8C3<> 8D8<
CPU_DATA<35>       6C8<> 8C3<> 8D8<
CPU_DATA<36>       6B8<> 8C3<> 8D8<
CPU_DATA<37>       6B8<> 8C3<> 8D8<
CPU_DATA<38>       6B8<> 8C3<> 8D8<
CPU_DATA<39>       6B8<> 8B3<> 8D8<
CPU_DATA<40>       6B8<> 8B3<> 8C8<
CPU_DATA<41>       6B8<> 8B3<> 8C8<
CPU_DATA<42>       6B8<> 8B3<> 8C8<

CPU_DATA<43>       6B8<> 8B3<> 8C8<
CPU_DATA<44>       6B8<> 8B3<> 8C8<
CPU_DATA<45>       6B8<> 8B3<> 8C8<
CPU_DATA<46>       6B8<> 8B3<> 8B8<
CPU_DATA<47>       6B8<> 8B3<> 8B8<
CPU_DATA<48>       6B8<> 8A8< 8B3<>
CPU_DATA<49>       6B8<> 8A8< 8B3<>
CPU_DATA<50>       6B8<> 8A8< 8B3<>
CPU_DATA<51>       6B8<> 8A8< 8B3<>
CPU_DATA<52>       6B8<> 8A8< 8B3<>
CPU_DATA<53>       6B8<> 8A8< 8B3<>
CPU_DATA<54>       6B8<> 8A8< 8B3<>
CPU_DATA<55>       6B8<> 8A8< 8B3<>
CPU_DATA<56>       6B8<> 8B3<> 8B3<>
CPU_DATA<57>       6B8<> 8B3<> 8B3<>
CPU_DATA<58>       6B8<> 8B3<> 8B3<>
CPU_DATA<59>       6B8<> 8B3<> 8B3<>
CPU_DATA<60>       6B8<> 8B3<> 8B3<>
CPU_DATA<61>       6B8<> 8B3<> 8B3<>
CPU_DATA<62>       6A8<> 8B3<> 8B3<>
CPU_DATA<63>       6A8<> 8B3<> 8B3<>
CPU_DBG_L          5C3< 8A3<> 8C2< 36D5>
CPU_DRDY_L         5C3> 8A3< 8C2< 36D5>
CPU_DTI<0>         5C3< 8A3<>
CPU_DTI<0..2>    36D5>
CPU_DTI<1>         5C3< 8A3<>
CPU_DTI<2>         5C3< 8A3<>
CPU_EDTI           5B2< 5C3<
CPU_EMODE0_L       5A3< 7A4<
CPU_EMODE1_L       5A3< 5C2<
CPU_GBL_L          5A7<> 8B5<> 36D5>
CPU_HIT_L          5A7> 8B5< 8D2< 36D5>
CPU_HRESET_INV     7A7<>
CPU_HRESET_L       5B3< 5C2< 6A1<> 7A5< 7A8< 39D6>
CPU_L1TSTCLK       5B2< 5B3<
CPU_L2TSTCLK       5B3< 5C2<
CPU_LSSD_MODE      5B3< 5C2<
CPU_MCP_L          5B3< 5D2<
CPU_PLL_CFG<0>     5C3< 7D3<
CPU_PLL_CFG<1>     5C3< 7D3<
CPU_PLL_CFG<2>     5C3< 7D3<
CPU_PLL_CFG<3>     5C3< 7D3<
CPU_PLL_CFG<4>     5C3< 7D3<>
CPU_PLL_CFGEXT     7D4<>
CPU_PLL_FS00       7C4<>
CPU_PLL_FS01       7C4<
CPU_PLL_FS10       7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC  7C4<> 7C8<> 29B6<>
CPU_PMONIN_L       5A3< 5C2<
CPU_PULLDOWN       5A2< 5A3< 5A3< 5C7<>
CPU_PULLUP         5A3< 5C2<
CPU_QACK_L         5B3< 8B5<> 36D5>
CPU_QREQ_L         5B3> 8B5< 8C2< 36D5>
CPU_SHD0_L         5A7<> 5D2<
CPU_SHD1_L         5A7<> 5D2<
CPU_SMI_L          5B3< 5C2< 29C4<>
CPU_SRESET_L       5B2< 5B3< 39D6>
CPU_SRWX_L         5A3< 5C2<
CPU_TA_L           5B3< 8A3<> 8D2< 36D5>
CPU_TBEN           5B3< 5D2< 8A5<>
CPU_TBST_L         5A7> 8B5<> 36D5>
CPU_TEA_L          5B3< 8A3<> 8C2< 36D5>
CPU_THERM_DM_SPN  25A6<
CPU_THERM_DP_SPN  25A6<
CPU_TSIZ<0>        5A7> 8B5<>
CPU_TSIZ<0..2>   36D5>
CPU_TSIZ<1>        5A7> 8B5<>
CPU_TSIZ<2>        5A7> 8B5<>
CPU_TS_L           5C7<> 8D2< 8D5<> 36D5>
CPU_TT<0>          5A7<> 8B5<>
CPU_TT<0..4>     36D5>
CPU_TT<1>          5A7<> 8B5<>
CPU_TT<2>          5A7<> 8B5<>
CPU_TT<3>          5A7<> 8B5<>
CPU_TT<4>          5A7<> 8B5<>
CPU_VCORE_HI_OC  7B8< 29D4<> 33C8< 33D7<
CPU_VCORE_PWR_SEQ  33D8<>
CPU_VCORE_SEQ      33D8<
CPU_VCORE_SEQ_L  33D8<
CPU_VCORE_SLEEP  5D2< 5D8<> 33C1< 33D2< 38D3> 39C6>

CPU_VCORE_SNUB     33B3<
CPU_WT_L           5A7> 8B5<> 36C5>
CSLOT_ADDR3_SPN  13B7>
CSLOT_ADDR4_SPN  13B7>
CSLOT_ADDR5_SPN  13B7>
CSLOT_ADDR6_SPN  13B7>
CSLOT_ADDR7_SPN  13B7>
CSLOT_ADDR8_SPN  13B7>
CSLOT_ADDR9_SPN  13B7>
CSLOT_CE1_L_SPN  13C7>
CSLOT_CE2_L_SPN  13C7>
CSLOT_IORD_L_SPN  13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN  13C7>
CSLOT_OE_L_SPN     13C7>
CSLOT_WE_L_SPN     13C7>
CURRENT_THRESHOLD  30C3<
CY25811_S0         19A4<
CY25811_S1         19A4<
DCDC_EN            20A7<> 28C8<> 32B7<> 33C7<>
DCDC_EN_L          32B6< 32B7<> 34C7<>
DDC_CLK_ISO        22D4<>
DDR_VREF           11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                 38D3>
DVI_DDC_CLK        22D4<>
DVI_DDC_CLK_UF     22C5<> 22D3<> 39B6>
DVI_DDC_DATA       22C4<>
DVI_DDC_DATA_UF  22C5<> 39B6>
DVI_HPD            22C4<>
DVI_HPD_DIV        22C3<
DVI_HPD_UF         22C3< 22C5<> 39B6>
DVI_TURN_ON        22D3<>
DVI_TURN_ON_BASE  22D2<>
DVI_TURN_ON_ILIM  22D2<
EIDE_ADDR<0>       13B7> 24B8<
EIDE_ADDR<2..0>  37B5>
EIDE_ADDR<1>       13B7> 24B8<
EIDE_ADDR<2>       13B7> 24B8<
EIDE_CS0_L         13B7> 24B8< 37B5>
EIDE_CS1_L         13B7> 24A8< 37B5>
EIDE_DATA<0>       13C7<> 24C8<
EIDE_DATA<15..0>  37B5>
EIDE_DATA<1>       13C7<> 24C8<
EIDE_DATA<2>       13C7<> 24C8<
EIDE_DATA<3>       13C7<> 24C8<
EIDE_DATA<4>       13C7<> 24B8<
EIDE_DATA<5>       13B7<> 24B8<
EIDE_DATA<6>       13B7<> 24B8<
EIDE_DATA<7>       13B7<> 24B8<
EIDE_DATA<8>       13B7<> 24D8<
EIDE_DATA<9>       13B7<> 24C8<
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EIDE_DATA<11>      13B7<> 24C8<
EIDE_DATA<12>      13B7<> 24C8<
EIDE_DATA<13>      13B7<> 24C8<
EIDE_DATA<14>      13B7<> 24C8<
EIDE_DATA<15>      13B7<> 24C8<
EIDE_DMACK_L       13A7<> 24A8< 37B5>
EIDE_DMARQ         13A7< 24A8< 37B5>
EIDE_INT           13A7< 24A8< 37B5>
EIDE_IOCHRDY       13B7< 24A8< 37B5>
EIDE_OPTICAL_ADDR<0>  24A5<> 24B7<
EIDE_OPTICAL_ADDR<2..0>  37B5> 39C3>
EIDE_OPTICAL_ADDR<1>  24A5<> 24B7<
EIDE_OPTICAL_ADDR<2>  24A6<> 24B7<
EIDE_OPTICAL_CS0_L  24A5<> 24B7< 37B5> 39C3>
EIDE_OPTICAL_CS1_L  24A6<> 24A7< 37B5> 39C3>
EIDE_OPTICAL_DATA<0>  24A5<> 24C7<
EIDE_OPTICAL_DATA<15..0>  37B5> 39C3>
EIDE_OPTICAL_DATA<1>  24A5<> 24C7<
EIDE_OPTICAL_DATA<2>  24A5<> 24C7<
EIDE_OPTICAL_DATA<3>  24A5<> 24C7<
EIDE_OPTICAL_DATA<4>  24A5<> 24B7<
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EIDE_OPTICAL_DATA<10>  24A6<> 24D7<
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EIDE_OPTICAL_DATA<13>  24A6<> 24C7<
EIDE_OPTICAL_DATA<14>  24A6<> 24C7<
EIDE_OPTICAL_DATA<15>  24A6<> 24C7<
EIDE_OPTICAL_DMAACK_L  24A6<> 24A7< 37A5> 39C3>
EIDE_OPTICAL_DMA_RQ  24A6<> 24A7< 37A5> 39C3>

EIDE_OPTICAL_INT  24A5<> 24A7< 37A5> 39B3>
EIDE_OPTICAL_IOCHRDY  24A5<> 24A7< 37A5> 39B3>
EIDE_OPTICAL_READ_L  24A6<> 24A7< 37B5> 39C3>
EIDE_OPTICAL_RST_L  24A7< 24B5<> 37A5> 39C3>
EIDE_OPTICAL_WR_L  24A5<> 24A7< 37B5> 39B3>
EIDE_RD_L          13A7> 24A8< 37B5>
EIDE_RST_L         13B7> 24A8< 37B5>
EIDE_WR_L          13A7> 24A8< 37B5>
ENET_COL           13C5< 26B7> 37A5>
ENET_COMA          26B7<>
ENET_CRS           13C5< 26B7> 37A5>
ENET_CTAP_CHGND  38A6>
ENET_ENERGY_DET  14B5<> 26B7<>
ENET_HSDACM        26A7<>
ENET_HSDACP        26A7<>
ENET_LINK_RXD<0>  13C5< 26C7>
ENET_LINK_RXD<7..0>  37A5>
ENET_LINK_RXD<1>  13C5< 26C7>
ENET_LINK_RXD<2>  13C5< 26C7>
ENET_LINK_RXD<3>  13C5< 26B7>
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ENET_LINK_RXD<6>  13C5< 26B7>
ENET_LINK_RXD<7>  13C5< 26B7>
ENET_LINK_TXD<0>  13B4< 13D5>
ENET_LINK_TXD<7..0>  37A5>
ENET_LINK_TXD<1>  13B4< 13D5>
ENET_LINK_TXD<2>  13B4< 13D5>
ENET_LINK_TXD<3>  13B4< 13D5>
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ENET_LINK_TXD<5>  13B4< 13D5>
ENET_LINK_TXD<6>  13A4< 13D5>
ENET_LINK_TXD<7>  13A4< 13D5>
ENET_LINK_TX_EN  13D5<> 37A5>
ENET_LINK_TX_ER  13D5<> 37A5>
ENET_MDC           13C5< 26B7< 37A5>
ENET_MDIO          13C5<> 26B7<> 37A5>
ENET_PHY_TXD<0>  13B5< 26C7<
ENET_PHY_TXD<7..0>  37A5>
ENET_PHY_TXD<1>  13B5< 26C7<
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ENET_PHY_TXD<6>  13A5< 26C7<
ENET_PHY_TXD<7>  13A5< 26C7<
ENET_PHY_TX_EN     13D6< 26C7< 37A5>
ENET_PHY_TX_ER     13D6< 26C7< 37A5>
ENET_RSET          26A5<
ENET_RST_L         26B7<
ENET_RX_DV         13D5< 26B7> 37A5>
ENET_RX_ER         13C5< 26B7> 37A5>
ENET_VSSC          26A7<>
ESP_EN_L           6C2<> 6C2<
FAN1_GND           38B6> 39A3>
FAN1_PWM           25A4<>
FAN1_PWM_L         25A4<> 25B2<>
FAN1_TACH          25A4< 25B2< 39A3>
FAN2_GND           38B6> 39A3>
FAN2_PWM           25A3<>
FAN2_PWM_L         25A3<> 25B2<>
FAN2_TACH          25A3< 25B2< 39A3>
FB_4_85V_BU        31A5<
FP_PWR_EN          20C6<> 22A5< 22B3<>
FP_PWR_EN_L        22B3<>
FWB_TPB0           27A3<
FWB_TPB1           27A3<
FWPLL_BYP          27D8<>
FW_BIAS0           27A4<>
FW_BIAS1           27A4<>
FW_BMODE           27B6<
FW_CORE_ADJ        27C7<
FW_CORE_BYP        27C7<>
FW_CPS             27B6<
FW_GATE_EN         28D6<>
FW_GATE_EN_RC      28C5<
FW_GATE_EN_UF      28C6<> 28C7<>
FW_INPUT_PD        27A6<
FW_LINK_CNTL<0>  13C3<> 27C3<
FW_LINK_CNTL<1..0>  37A5>
FW_LINK_CNTL<1>  13C3<> 27C3<
FW_LINK_DATA<0>  13D3<> 27B7<
FW_LINK_DATA<7..0>  37A5>
FW_LINK_DATA<1>  13D3<> 27B7<
FW_LINK_DATA<2>  13D3<> 27B7<
FW_LINK_DATA<3>  13D3<> 27B7<
FW_LINK_DATA<4>  13C3<> 27B7<
FW_LINK_DATA<5>  13C3<> 27A7<
FW_LINK_DATA<6>  13C3<> 27A7<
FW_LINK_DATA<7>  13C3<> 27A7<
FW_LINK_LREQ       13C3<> 37A5>
FW_LKON            13C3<> 27B4<>
FW_LT1641_FB       28D6<
FW_OSC             27A4< 35A1>
FW_OSC_EN          27A3<
FW_PC_PD           27B6<
FW_PC_PU           27B6<
FW_PHY_CNTL<0>   27B4<> 27C4<
FW_PHY_CNTL<1..0>  37A5>
FW_PHY_CNTL<1>   27B4<> 27C4<
FW_PHY_DATA<0>   27B7<>
FW_PHY_DATA<7..0>  37A5>
FW_PHY_DATA<1>   27B7<>
FW_PHY_DATA<2>   27B7<>
FW_PHY_DATA<3>   27B7<>
FW_PHY_DATA<4>   27B7<>
FW_PHY_DATA<5>   27A7<>
FW_PHY_DATA<6>   27A7<>
FW_PHY_DATA<7>   27A7<>
FW_PHY_LPS         13C3<> 27B7<
FW_PHY_LREQ        13C2< 27B7< 37A5>
FW_PHY_PD          14C5<> 27B7<
FW_PHY_RESET_L   27A7<
FW_PINT            13C3<> 27B4> 37A5>
FW_PLL_ADJ         27C7<
FW_PORT1_SEL       27B6<
FW_POWER_UP        28D8<>
FW_PWR_UP_DIV      28C7<
FW_R0              27A4<>
FW_R1              27A4<>
FW_TESTM           27A6<
FW_TIMER           28C7<
FW_TPA1N           27B2<> 28A4<> 37D2>
FW_TPA1P           27B2<> 28A4<> 37D2>
FW_TPB1N           27A2<> 28A4<> 37D2>
FW_TPB1P           27B2<> 28A4<> 37D2>
FW_TPB2_PD         27A4<>
FW_TPI0N           27B2<> 28C2<> 28C3<> 37D2> 39A3>
FW_TPI0P           27B2<> 28C2<> 28C3<> 37D2> 39A3>
FW_TPI1N           28A3<> 37D2> 39D1>
FW_TPI1P           28A3<> 37D2> 39D1>
FW_TPO0N           27B2<> 28C2<> 28C3<> 37D2> 39A3>
FW_TPO0P           27B2<> 28C2<> 28C3<> 37D2> 39A3>
FW_TPO0R           28C1<> 39A3>
FW_TPO1N           28A3<> 37D2> 39D1>
FW_TPO1P           28A3<> 37D2> 39D1>
FW_VCC_ON          28D7<>
FW_VCC_ON_DIV      28D7<
FW_VCC_ON_GATE_L  28D7<>
FW_VDD_ON          38A3>
FW_VGND            39A3> 39D1>
FW_VGND0           28C1<> 38A3>
FW_VGND1           28A3<> 38A3>
FW_VREG_PD         27A6<
FW_XI              27A4<> 35A1>
GPU_AGP_TEST       19C6<
GPU_B              20D6<> 22C8<
GPU_B_FILTR        22C8<
GPU_C              20D6<> 22A8<
GPU_COMP           20D6<> 22A8<
GPU_CORE_OK        20A6<> 20D4<> 21D2<> 21D7<>
GPU_DVI_DDC_CLK  20C5<> 22D3<>
GPU_DVI_DDC_DATA  20C5<> 22C3<>
GPU_DVOD<0>        19B3< 19C4<
GPU_DVOD<11..0>  36C1>
GPU_DVOD<1>        19B3< 19C4<
GPU_DVOD<2>        19B3< 19C4<
GPU_DVOD<3>        19B3< 19C4<
GPU_DVOD<4>        19B3< 19C4<
GPU_DVOD<5>        19B3< 19C4<
GPU_DVOD<6>        19B3< 19C4<
GPU_DVOD<7>        19B3< 19C4<
GPU_DVOD<8>        19B2< 19C4<
GPU_DVOD<9>        19B2< 19C4<
GPU_DVOD<10>       19B2< 19C4<
GPU_DVOD<11>       19B2< 19C4<
GPU_DVOD_DE        19B2< 19C4< 36C1>
GPU_DVO_CLKP       19B2< 19C4< 36C1>

GPU_DVO_HSYNC      19B2< 19C4< 36C1>
GPU_DVO_VSYNC      19B2< 19C4< 36C1>
GPU_G              20D6<> 22C8<
GPU_G_FILTR        22C8<
GPU_HPD            20C5< 22C3<>
GPU_MEM_IO         19A6<> 19B8< 21A7< 21B4< 21D2<
                 38C3>
GPU_MEM_IO_FLT     21C2< 38C3>
GPU_R              20D6<> 22B8<
GPU_R_FILTR        22B8<
GPU_THERM_DM       19A6<> 25A6<
GPU_THERM_DP       19A6<> 25A6<
GPU_TMDS_CLKN      19B2< 20B8< 20D7< 36D1>
GPU_TMDS_CLKP      19B2< 20B8< 20D8< 36D1>
GPU_TMDS_CLK_CMF  20D7<
GPU_TMDS_D0_CMF  20D7<
GPU_TMDS_D1_CMF  20C7<
GPU_TMDS_D2_CMF  20C7<
GPU_TMDS_DN<0>     19B2< 20B8< 20D7< 36D1>
GPU_TMDS_DN<1>     19B2< 20B8< 20C7< 36D1>
GPU_TMDS_DN<2>     19A2< 20B8< 20C7< 36D1>
GPU_TMDS_DP<0>     19B2< 20B8< 20D8< 36D1>
GPU_TMDS_DP<1>     19B2< 20B8< 20C8< 36D1>
GPU_TMDS_DP<2>     19A2< 20B8< 20C8< 36D1>
GPU_TV_GND1        22B8<> 38B6>
GPU_TV_GND2        22A8<> 38B6>
GPU_VCORE          19D8< 20A3<> 20B5<> 20D4< 38C3>
                 39C6>
GPU_VCORE_CNTL     20A3<>
GPU_VCORE_CNTL_L  20A4< 20B7<>
GPU_VCORE_CNTL_RC  20A3<>
GPU_VCORE_NECK     20B5<> 38B3>
GPU_VCORE_PWR_SEQ  20A8<>
GPU_VCORE_SEQ      20A8<
GPU_VCORE_SEQ_L  20A8<
GPU_VCORE_SW       20A4<> 38B1>
GPU_VCORE_SW_F     20A3<> 38B1>
GPU_VCORE_VDDCI  19C8< 19D6< 38B3>
GPU_Y              20D6<> 22B8<
HD_ADDR<0>         24C2<> 24C3<
HD_ADDR<2..0>    37C5>
HD_ADDR<1>         24C2<> 24C3<
HD_ADDR<2>         24B3< 24C1<>
HD_CS0_L           24C2<> 24C3< 37B5>
HD_CS1_L           24B3< 24C1<> 37B5>
HD_DATA<0>         24C2<> 24D3<
HD_DATA<15..0>   37C5>
HD_DATA<1>         24C2<> 24D3<
HD_DATA<2>         24D2<> 24D3<
HD_DATA<3>         24D2<> 24D3<
HD_DATA<4>         24C3< 24D2<>
HD_DATA<5>         24C3< 24D2<>
HD_DATA<6>         24C3< 24D2<>
HD_DATA<7>         24C3< 24D2<>
HD_DATA<8>         24C3< 24D1<>
HD_DATA<9>         24C3< 24D1<>
HD_DATA<10>        24C3< 24D1<>
HD_DATA<11>        24D1<> 24D3<
HD_DATA<12>        24B3< 24D1<>
HD_DATA<13>        24B3< 24D1<>
HD_DATA<14>        24C1<> 24C3<
HD_DATA<15>        24B3< 24C1<>
HD_DIOR_L          24A3< 24C2<> 37B5>
HD_DIOW_L          24A3< 24C1<> 37B5>
HD_DMACK_L         24A3< 24C2<> 37B5>
HD_DMARQ           13C6< 24C2<> 37B5>
HD_INTRQ           13C6< 24C1<> 37B5>
HD_IOCHRDY         24A3< 24C1<> 37B5>
HD_RESET_L         24A3< 24D2<> 37C5>
HIGH_VCORE         20A2<>
HIGH_VCORE_DIVD  20A3<
HPD_4V_REF         22C3<
HPD_PWR_SNS_EN     20C7<> 22C3<>
HPD_PWR_SW         22C2<
HPD_PWR_SW_BASE  22C2<>
HPD_REF_EN_L       22C2<>
IAC_FB             30D3<
IAC_RC_COMP        30D3<
ICT_TRST_L         6B2<> 6C2<
INTREPID_ACS_REF  8A5<
INT_AGPPVT         12D4<>
INT_AGP_FB_IN      12C4< 35C1>
INT_AGP_FB_OUT     12C4<> 35C1>
INT_AGP_VREF       12B5< 12D4<> 19D6< 38C3>
INT_CPUFB_IN       8A5< 8B5< 35D1>
INT_CPUFB_IN_NORM  8A4< 35D1>
INT_CPUFB_LONG     8A3< 35D1>
INT_CPUFB_OUT      8A5<> 8A5< 35D1>
INT_CPUFB_OUT_NORM  8A4< 35D1>
INT_CPUFB_OUT_SHORT  8A5< 35D1>
INT_DDRCLK2_N_TP  9B6<>
INT_DDRCLK2_P_TP  9B6<>
INT_DDRCLK5_N_TP  9B6<>
INT_DDRCLK5_P_TP  9B6<>
INT_ENET_RST_L     14B5<> 26B8<
INT_EXTINT3_PU     14A7< 14B5<>
INT_EXTINT8_PU     14B5<> 14C7<
INT_EXTINT10_PU  14B5<> 14B7<
INT_EXTINT11_PU  14B5<> 14B7<
INT_EXTINT12_PU  14B5<> 14B7<
INT_EXTINT13_PU  14B5<> 14B7<
INT_EXTINT14_PU  14B5<> 14C7<
INT_EXTINT16_PU  14B5<> 14B7<
INT_GPIO1_PU       14A7< 14C5<> 33C8<
INT_GPIO9_PU       14A7< 14B5<>
INT_GPIO12_PU      14B5<> 14B7<
INT_GPIO15_PU      14B5<> 14B7<
INT_I2C_CLK0       6B3<> 6D2< 11A5<> 11A8<> 13C2<
                 13C3<> 23D7<> 39C6>
INT_I2C_CLK1       13C2< 13C3<> 14B7< 25B4< 39C6>
INT_I2C_CLK2       14A2<> 25C4<> 25D7<> 39A6>
INT_I2C_DATA0      6B3<> 6D2<> 11A5<> 11A8<> 13C2<
                 13C3<> 23D7<> 39C6>
INT_I2C_DATA1      13B2< 13C3<> 14B7< 25B4<> 39C6>
INT_I2C_DATA2      14A2<> 25D4<> 25D7<> 39A6>
INT_I2S0_SND_FROM_ADC  14B2< 25D7<> 39A6>
INT_I2S0_SND_LRCLK  14B1< 25D8<> 39A6>
INT_I2S0_SND_LRCLK_UF  14A3<>
INT_I2S0_SND_MCLK  14B1< 25D8<> 35B1> 39A6>
INT_I2S0_SND_MCLK_UF  14A3<>
INT_I2S0_SND_SCLK  14B1< 25D7<> 39A6>
INT_I2S0_SND_SCLK_UF  14A3<>
INT_I2S0_SND_TO_DAC  14B1< 25D8<> 39A6>
INT_I2S0_SND_TO_DAC_UF  14B3<>
INT_JTAG_TEI       13C2< 13C5< 39D6>
INT_MEM_REF_H      9B6< 38C3>
INT_MEM_VREF       9A7< 9B6<> 38C3>
INT_MOD_BITCLK     14A1< 25D3<>
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT     14A1< 25D4<>
INT_MOD_CLKOUT_UF  14A3<> 14A7<
INT_MOD_DTI        14A2< 14A7< 25D3<>
INT_MOD_DTO        14B1< 25D4<>
INT_MOD_DTO_UF     14A3<> 14A7<
INT_MOD_SYNC       14A1< 25D3<>
INT_MOD_SYNC_UF  14A3<> 14A7<
INT_PCI_FB_IN      12C7< 35C1>
INT_PCI_FB_OUT     12C7<> 35C1>
INT_PEND_PROC_INT  14A5> 29C4<>
INT_PROC_SLEEP_REQ_L  14A5< 29B4<>
INT_PU_RESET_L     13D3< 25D5<> 29A2< 29C4<>
INT_REF_CLK_IN     14A5< 14B5< 35C1>
INT_REF_CLK_OUT  14A5< 14B7< 35C1>
INT_REF_CLK_OUT_UF  14A5<> 35C1>
INT_RESET_L        9B3< 13D3< 29C7< 29D4<>
INT_ROM_CS_L       12A5< 12C7>
INT_ROM_OE_L       12A5< 12C7>
INT_ROM_RW_L       12A5< 12C7>
INT_SUSPEND_ACK_L  8B5> 29B6<>
INT_SUSPEND_REQ_L  8B5< 29B6<> 29C7<
INT_TST_MONIN_PD  13C2< 13C5< 39C6>
INT_TST_MONOUT_TP  13C5> 39C6>
INT_TST_PLLEN_PD  13C5< 13D2< 39C6>
INT_WATCHDOG_L     14A5> 29C6<>
INV_GND            22A1<> 39A6>
INV_ON_PWM         20C6<> 22A3<
IO_RESET_L         17A8< 23D7<> 26B8< 29C6<> 29D7<
JTAG_ASIC_TCK      13C5< 13D2< 26A5< 39D6>
JTAG_ASIC_TDI      13C5< 13D2< 39D6>
JTAG_ASIC_TDO_TP  26A5> 39D6>
JTAG_ASIC_TMS      13C5< 13D2< 26A5< 39D6>
JTAG_ASIC_TRST_L  13C5< 13D2< 26A5< 39D6>
JTAG_CPU_TCK       5B2< 5B3< 6A3> 39D6>
JTAG_CPU_TDI       5B2< 5C3< 6B2<> 39D6>
JTAG_CPU_TDO_TP  5C3> 39D6>
JTAG_CPU_TMS       5B2< 5B3< 6B2<> 39D6>
JTAG_CPU_TRST_L  5A3< 5B3< 6B2<> 39D6>
JTAG_ENET_TDI      13C5> 13D2< 26A5<

KBD_CAPSLOCK_LED  23C1<> 39B3>
KBD_COMMAND_L      23A2< 23C1<> 29C6<> 39B3>
KBD_CONTROL_L      23B2< 23C1<> 29A8< 29C6<> 39A3>
KBD_FUNCTION_L     23A2< 23C1<> 29B6<> 39B3>
KBD_ID             23B2< 23C1<> 29B6<> 39B3>
KBD_INTL           23C1<> 39B3>
KBD_JIS            23C1<> 39B3>
KBD_LED1_OUT       23B5<> 23D7<>
KBD_LED2_OUT       23B4<> 23D7<>
KBD_NUMLOCK_LED  23C1<> 39B3>
KBD_OPTION_L       23A2< 23C1<> 29A8< 29B6<> 39B3>
KBD_SHIFT_L        23A2< 23C1<> 29A8< 29C6<> 39A3>
KBD_X<0>           23B2< 23C1<> 29C6<>
KBD_X<0..9>      39A3>
KBD_X<1>           23B2< 23C1<> 29C6<>
KBD_X<2>           23B2< 23C1<> 29C6<>
KBD_X<3>           23B2< 23C1<> 29C6<>
KBD_X<4>           23B2< 23C1<> 29C6<>
KBD_X<5>           23B2< 23C1<> 29C6<>
KBD_X<6>           23B2< 23D1<> 29C6<>
KBD_X<7>           23B2< 23D1<> 29C6<>
KBD_X<8>           23A2< 23D1<> 29C6<>
KBD_X<9>           23A2< 23D1<> 29C6<>
KBD_Y<0>           23D1<> 29D6<>
KBD_Y<0..7>      39A3>
KBD_Y<1>           23D1<> 29D6<>
KBD_Y<2>           23D1<> 29D6<>
KBD_Y<3>           23D1<> 29D6<>
KBD_Y<4>           23D1<> 29D6<>
KBD_Y<5>           23D1<> 29C6<>
KBD_Y<6>           23D1<> 29C6<>
KBD_Y<7>           23D1<> 29C6<>
LCD_DIGON_L        22B6<
LCD_PWREN_L        22B5<>
LED_LINK10         26B5<>
LED_LINK100        26B5<>
LED_RX_SPN         26B5>
LID_CLOSED_L       23B4<> 39B3>
LM2594_IN          27D8<> 38A3>
LMU_DETECT         23C7< 23D6<> 39D1>
LT1962_INT_ADJ   14D7<
LT1962_INT_BYP   14D7<>
LTC1625_ITH        30D2<>
LTC1962_INT_VIN  14D8<> 38A1>
LTC3405_SW         26D4<> 38A3>
LTC3411_EN_L       34A7<
LTC3411_GND        34A5<> 38A1>
LTC3411_ITH        34A5<> 38A1>
LTC3411_ITH_RC     34A5< 38A1>
LTC3411_SHDN       34A6<> 38A1>
LTC3411_SYNC       34A6<> 38A1>
LTC3411_VCC        34A6< 34A7< 38B1>
LTC3707_START_RC  32B6<
LUX_ALS_GAIN_SW  23B7<> 23D6<>
LUX_ALS_OUT        23B7<> 23D6<>
LVDS_DDC_CLK       20C5<> 22A4< 22B4<> 39B6>
LVDS_DDC_DATA      20C5<> 22A4< 22B4<> 39B6>
LVDS_L0N           20B5> 22B4<> 37C2> 39B6>
LVDS_L0P           20B5> 22B4<> 37C2> 39B6>
LVDS_L1N           20B5> 22B4<> 37C2> 39B6>
LVDS_L1P           20B5> 22B4<> 37C2> 39B6>
LVDS_L2N           20B5> 22A4<> 37C2> 39B6>
LVDS_L2P           20B5> 22A4<> 37C2> 39B6>
LVDS_L3N_TP        20B5>
LVDS_L3P_TP        20B5>
LVDS_U0N           20C5> 22A4<> 37C2>
LVDS_U0P           20C5> 22A4<> 37C2>
LVDS_U1N           20C5> 22A4<> 37C2>
LVDS_U1P           20C5> 22A4<> 37C2>
LVDS_U2N           20B5> 22A4<> 37C2>
LVDS_U2P           20B5> 22A4<> 37C2>
LVDS_U3N_TP        20B5>
LVDS_U3P_TP        20B5>
MAIN_RESET_L       14C7< 17A8< 18A7< 19B8< 19D4<
                 24D6<> 29D4<> 29D7< 39C3>
MAX1715_GND        34B5<> 34C5< 38C1>
MAX1715_ON_RC      34C7<>
MAX1715_REF        34B5<> 38C1>
MAX1715_SKIP       34C4< 38C1>
MAX1715_TON        34C5< 38C1>
MAX1715_VCC        34D5< 38C1>
MAX4172_OUT        30D4<>
MAXBUS_SLEEP       5A2< 5D2< 5D5< 6B2< 6B4< 7B7< 7D8<
                 8B3< 8B8< 8C8< 8D1< 8D8< 15D8< 16D8<
                 33D8< 38D3>
MDI0_PD            26B4<
MDI1_PD            26B4<
MDI2_PD            26B4<
MDI3_PD            26B3<
MDI_M<0>           26B5<> 37D2>
MDI_M<0..3>      39A3>
MDI_M<1>           26B5<> 37D2>
MDI_M<2>           26B5<> 37C2>
MDI_M<3>           26B5<> 37C2>
MDI_P<0>           26B5<> 37D2>
MDI_P<0..3>      39A3>
MDI_P<1>           26B5<> 37D2>
MDI_P<2>           26B5<> 37C2>
MDI_P<3>           26B5<> 37C2>
MEM_ADDR<0>        9B5< 9D6<>
MEM_ADDR<12..0>  35A5>
MEM_ADDR<1>        9B5< 9D6<>
MEM_ADDR<2>        9B5< 9D6<>
MEM_ADDR<3>        9B5< 9D6<>
MEM_ADDR<4>        9B5< 9D6<>
MEM_ADDR<5>        9B5< 9D6<>
MEM_ADDR<6>        9B5< 9D6<>
MEM_ADDR<7>        9B5< 9D6<>
MEM_ADDR<8>        9B5< 9D6<>
MEM_ADDR<9>        9A5< 9D6<>
MEM_ADDR<10>       9A5< 9D6<>
MEM_ADDR<11>       9A5< 9D6<>
MEM_ADDR<12>       9A5< 9D6<>
MEM_BA<0>          9A5< 9D6<>
MEM_BA<1..0>     35A5>
MEM_BA<1>          9A5< 9C6<>
MEM_CAS_L          9A5< 9C6<> 35A5>
MEM_CKE<0>         9B6<> 9C5<
MEM_CKE<3..0>    35A5>
MEM_CKE<1>         9B6<> 9C5<
MEM_CKE<2>         9B6<> 9C5<
MEM_CKE<3>         9B6<> 9C5<
MEM_CS_L<0>        9C5< 9C6<>
MEM_CS_L<3..0>   35A5>
MEM_CS_L<1>        9C5< 9C6<>
MEM_CS_L<2>        9C5< 9C6<>
MEM_CS_L<3>        9C5< 9C6<>
MEM_DATA<0>        9D8<> 10C7<>
MEM_DATA<7..0>   35D5>
MEM_DATA<1>        9D8<> 10C7<>
MEM_DATA<2>        9D8<> 10C7<>
MEM_DATA<3>        9D8<> 10C7<>
MEM_DATA<4>        9D8<> 10C7<>
MEM_DATA<5>        9D8<> 10C7<>
MEM_DATA<6>        9D8<> 10C7<>
MEM_DATA<7>        9D8<> 10C7<>
MEM_DATA<8>        9D8<> 10C7<>
MEM_DATA<15..8>  35D5>
MEM_DATA<9>        9D8<> 10C7<>
MEM_DATA<10>       9D8<> 10C7<>
MEM_DATA<11>       9D8<> 10C7<>
MEM_DATA<12>       9D8<> 10B7<>
MEM_DATA<13>       9C8<> 10B7<>
MEM_DATA<14>       9C8<> 10B7<>
MEM_DATA<15>       9C8<> 10B7<>
MEM_DATA<16>       9C8<> 10C5<>
MEM_DATA<23..16>  35C5>
MEM_DATA<17>       9C8<> 10C5<>
MEM_DATA<18>       9C8<> 10C5<>
MEM_DATA<19>       9C8<> 10C5<>
MEM_DATA<20>       9C8<> 10C5<>
MEM_DATA<21>       9C8<> 10C5<>
MEM_DATA<22>       9C8<> 10C5<>
MEM_DATA<23>       9C8<> 10C5<>
MEM_DATA<24>       9C8<> 10C5<>
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MEM_DATA<26>       9C8<> 10C5<>
MEM_DATA<27>       9C8<> 10C5<>
MEM_DATA<28>       9C8<> 10C5<>
MEM_DATA<29>       9C8<> 10B5<>
MEM_DATA<30>       9C8<> 10B5<>
MEM_DATA<31>       9C8<> 10B5<>
MEM_DATA<32>       9C8<> 10C3<>
MEM_DATA<39..32>  35C5>
MEM_DATA<33>       9C8<> 10C3<>
MEM_DATA<34>       9C8<> 10C3<>
MEM_DATA<35>       9C8<> 10C3<>

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MEM_DATA<40>       9B8<> 10C3<>
MEM_DATA<47..40>  35B5>
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MEM_DQS<1>         9C6<> 10B7<> 35D5>
MEM_DQS<2>         9C6<> 10C5<> 35C5>
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MEM_DQS<7>         9C6<> 10B1<> 35A5>
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MEM_MUXSEL_MSB     9B6<> 10B1<> 10B3<> 35A5>
MEM_MUXSEL_MSB_L_TP  9B6<>
MEM_RAS_L          9A5< 9C6<> 35A5>
MEM_WE_L           9A5< 9C6<> 35A5>
MODEM_USB_DM       14B1< 25D3<> 37B2> 39D3>
MODEM_USB_DP       14C1< 25D3<> 37B2> 39D3>
MPIC_CPU_INT_L     5B2< 5B3< 14B5>
NEC_AMC_TP         17A5<
NEC_AVDD           17D5< 38A3>
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NEC_LUSB_PPON      17B5> 25D8<> 39A6>
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NEC_USB_DBM        17C2<> 25D2<> 37B2> 39D3>
NEC_USB_DBP        17C2<> 25D2<> 37A2> 39D3>
NEC_USB_RSDM1      17C5<>
NEC_USB_RSDM2      17C5<>
NEC_USB_RSDP1      17C5<>
NEC_USB_RSDP2      17C5<>
NEC_XT1            17D5<
NEC_XT2            17D5<>
NEC_XT2_R          17D4<
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NUMLOCK_LED_L      23D2< 29C7<
OVER_18V_ADJ       30C3<>
PCI1510_VR_EN_L  18C7<
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PMU_BATT1_DET_L_PU  29B4<> 29D2<
PMU_BATT_DET_L   29B3< 29D2< 30A4<> 39A3>
PMU_BYTE           29B6<> 29C7<
PMU_CAPSLOCK_LED_L  29C6<>
PMU_CHARGE_V       29C4<> 30B8<>
PMU_CHRG_BATT_0  29C4<> 30A8<>
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PMU_CNVSS        29B6< 29C7<
PMU_CPU_HRESET_L  6A2< 6C3<> 29C4<> 39C1>
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PMU_I2C_DATA     29B4<> 29C2<
PMU_INT_L        14B5<> 14B7< 29B6<>
PMU_INT_NMI      14B5<> 14B7< 29D4<>
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PMU_KB_RESET_IN2  29A7<>
PMU_KB_RESET_L   29A6> 29B7< 39C1>
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PMU_NMI_BUTTON_L  29C2< 29C4<>
PMU_NMI_L        29C2< 29C4<>
PMU_NUMLOCK_LED_L  29C6<>
PMU_OOPS         29B2< 29B4<>
PMU_PME_L        14A5<> 17A8< 24D5<> 29B2< 29C4<>
                 39C3>
PMU_POWERUP_OK   29B4<> 29D2<
PMU_POWER_UP_L   28C8<> 29C6<> 29D7< 32B8<
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PMU_SLEEP_LED_L  23C8<> 29C4<>
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RAM_ADDR<5>      9B4< 11B5<> 11B8<>
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RAM_DATA_A<7..0>  35D5>
RAM_DATA_A<1>    10C8<> 11D8<>
RAM_DATA_A<2>    10C8<> 11D8<>
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RAM_DATA_A<40>   10B4<> 11B8<>
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RAM_DATA_A<48>   10C2<> 11A8<>
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RAM_DATA_A<52>   10B2<> 11A6<>
RAM_DATA_A<53>   10B2<> 11A6<>
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*** Part Cross-Reference for the entire design ***

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J3	CON_M40ST_D4MT_SM	25
J4	CON_4RT_WRIB	22
J5	CON_M80ST_D4MT_SM	18
J6	CON_F80ST_D4MT_SM	24
J7	CON_12	33
J8	CON_2RTSM_125	23
J9	CON_F1ST_S2MT_SM	14
J10	CON_10STSM_5087	23
J11	CON_F30RT_S2MT_SM1	23
J12	CON_M50SM_5MM	24
J13	CON_M50SM_5MM	24
J14	CON_F30RT_S2MT_SM	22
J15	CON_M16ST_D_SMA	25
J16	CON_3RTSM_125	31
J17	CON_M16ST_D_SMA	25
J18	CON_M4RT_S2MT_SM	25
J19	CON_F20ST_D_SM	23
J20	CON_F9RT_1394B_S6MT_SMA	28
J21	CON_F5RT_MINIDIN_TH	22
J22	CON_F30RT_T6MT_TH1	22
J23	CON_RJ45_10RT_S4MT_TH1	26
J24	CON_F6RT_S4MT_TH1	28
J25	CON_F400RT_DDRDIMM_SM3	11
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